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Design of Hybrid multi-level inverter for photovoltaic(PV) application

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Abstract **–** Nowadays the demand and consumption of energy increase in the word. Due to high cost of fossil fuel it's not able to meet the required power generation demand. But the developed and developing countries encourage to generate power from renewable energy sources. The developed countries manage their resources in such a manner that they will fulfill their needs today and in the future as well. Nevertheless, the developing countries have limited sources of fossil fuels, which may decrease day by day. For this problem, the alternate solution is required, which is renewable energy. The output of renewable i.e. photovoltaic (PV) is DC. Now this is a challenging task for the researcher to integrate the renewable energy into the ac grid. For the reliable future of the power system, it is imperative for the modern era to integrate non-conventional sources into the AC power grid.

The use of photovoltaic cells is increasing dramatically in all areas of life because of their small environmental impact, pollution-free, minimal maintenance, and zero noise. The real work focuses on the integration of PV systems with the proposed new topology called Multi-level inverters based on switch dc sources for low, medium and high power applications. An inverter is a power electronics device that converts DC input to AC output voltage. Input DC voltage is obtains from PV cell array, fuel cell or any other source.

The output of PV panels is use as DC input voltage source for the proposed inverter. Single-phase multi-level inverter is use to convert dc power receiving form PV array to AC power. First single phase two level inverter introduce which have many problems like those that high value capacitor required at output and high total harmonics distortion's (THD). Nevertheless, as the number of level increased in inverter output the number of electronic switches also increased which may increase the losses.

Multi-level inverters are gave more attention for high power applications. In recent years, lower order harmonic components has been developed to operate at higher switching frequencies.On the other side as the number of level increased the output waveform approach to sinusoidal waveform and the harmonics decreased. Output voltage and current waveforms are obtains and THDs are analyze. The multi-level inverter used in un-interrupted power supply (UPS), variable frequency drives (VFD), pumps etc. The performance of single-phase multi-level inverter will be analyzed in MATLAB / Simulink software.

Keywords – PV, THD etc

I. INTRODUCTION

Nowadays multi-level inverter plays a vital rule in different areas like photovoltaic system, electric vehicles, grid integration system and low power load. Multi-level inverter is more attractive to the researcher's due to its low distortion, low power losses, absence of filter, low voltage stresses, low number of drivers and switching losses.

The recent development in power electronics enables the researcher to produce more energy

form non-conventional sources. The more non-conventional source of energy is solar cell (PV) and wind energy [1] [10]. The solar cell converts sun radiation direct into electrical energy, which has no moving part and an easy way to produce energy [3 4]. It is environmental friendly, because it cannot produce any pollution in air. Its installation and connection are easy and cannot require any expert. It is easily available in local market and can be handling easily. Its price is low and can be bought by any person of the society. Production of electrical energy is easy at low and domestic level, because a person can install his own plant at home. Due to this significance, the usage of solar cell energy production increases nowadays [1] [6]. The solar system can install in the area, which is away from the national grid. Solar cells can be interconnected either in series or in parallel, depending on the specified requirements of the users [1]. The solar system is the combination of solar cell, batteries (if required) and inverter. Inverters are the most complex and important part of the solar system, which is select carefully. Inverters are categorized in single phase and three phase inverters [3]. In low power application, square wave is reasonable, and in high power application, sine wave with small distortion is required [3]. A traditional two-level inverter has high THD and dv/dt output. A multi-level inverter can mitigate these drawbacks [6][9].

Now we need multi-level inverters (MLI) to convert solar cell DC output to AC output [2]. Multi-level inverters produce smoother output waveforms than two-level inverters. This new topology has some offer advantages in terms of generating high output voltage, low switching losses, and low distortion in the current waveform. With the development of semiconductors, this attractive feature has led to the interface between renewable energy and the utility grid [7 12].

The multi-level inverter is highly recommended as the optimal choice for medium and high voltage application. [4]

The MLI make it possible to integrate non-conventional energy to the power grid. MLI has three configurations [2-5].

Diode clamped multilevel inverter

Flying capacitor (FC)

Cascaded H-bridge (CHB)

Due to simplicity, the CHB is use nowadays. Any number of levels can be obtaining from H-bridge cascade topology.

II. PROPOSED SYSTEM

In recent time hybrid cascade inverters are under consideration. Which generate staircase voltage level with low switches count. The following points can summarize the main contribution of the proposed topology.

1. The proposed topology inherits the advantageous features of both H bridge type MLI and PUC MLI. This hybridization has allowed the H bridge type MLI to reduce the total voltage stress as well as produce higher voltage levels using fewer components.

2. H-Bridge and PUC inverters are cascaded.

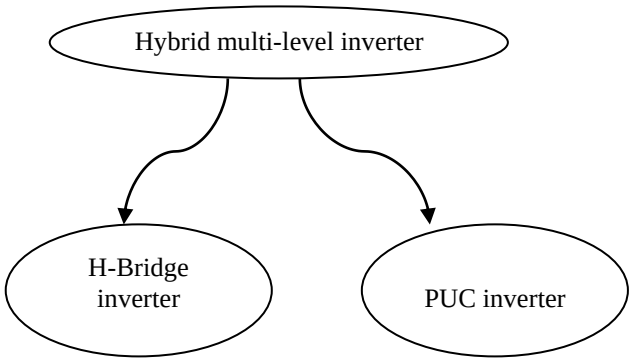


Fig 1 H-Bridge and PUC inverters

(a) H-Bridge inverter

The H-bridge consist four semiconductor switches from S1 to S4 and voltage source of Vdc. These switches are high voltage low frequency switches and generate three level output waveform, which is the input of PUC inverter.

Table.1:- 3-level H-bridge MLI switching table

Switching states				Output voltage
Qa	Qb	Qc	Qd	
1	0	1	0	+Vdc
0	1	1	0	0
0	1	0	1	-- Vdc

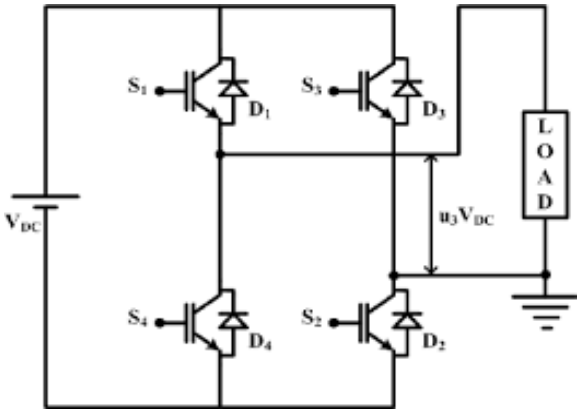


Fig 2 H-bridge inverter

(b) PUC inverter

The PUC inverter consists of six semiconductor switches from Q1 to Q6 with two voltage sources of Vdc/2. These switches are low voltage high frequency switches. PUC inverter generate 5 level output waveform, which is show in Fig 4(b) The output contains 9 levels of ± 2Vdc, ± 3/2Vdc, ± Vdc, ± 1/2Vdc and 0 Vdc.

Table.2:- 5-level PUC MLI switching table

Mode	Q1	Q2	Q3	Q4	Q5	Q6	Vbc
1	1	0	0	1	0	1	+2Vdc
2	0	1	0	1	1	0	+Vdc
3	1	0	1	0	1	0	0 Vdc
4	1	0	1	0	0	1	-Vdc
5	0	1	1	0	1	0	-2Vdc

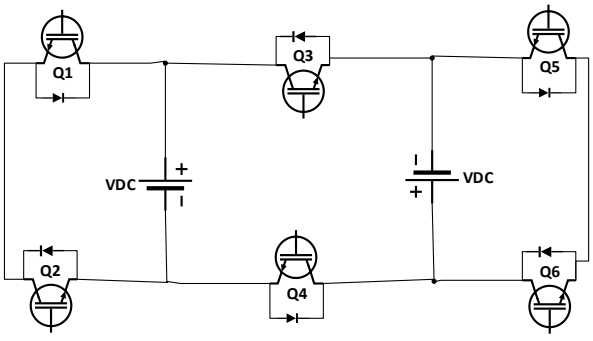


Fig 3 PUC inverter

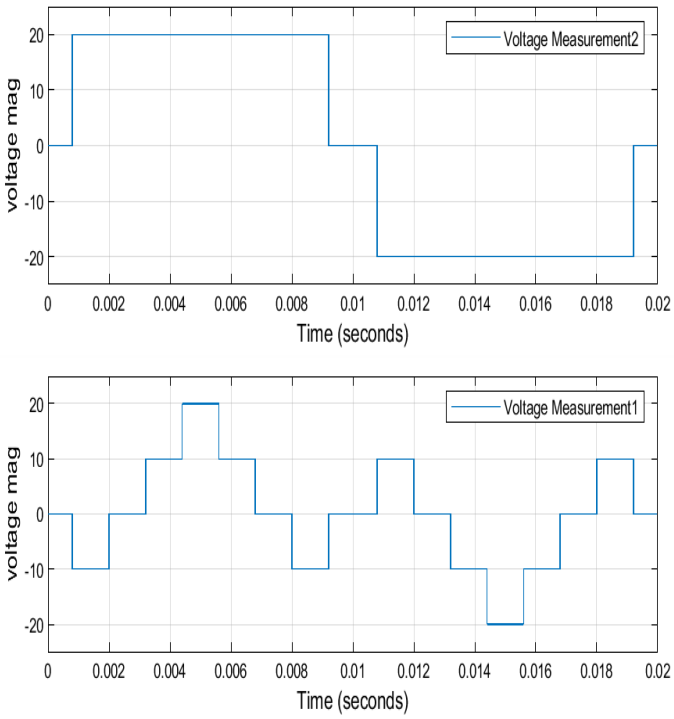


Fig 4 (a) waveform plot for H-bridge (b) waveform plot for PUC

(c) Proposed HMLI multi-level inverter topology

When the above two inverter are cascaded in series a new hybrid multi-level inverter topology are formed. It will produce 9 levels waveform at the output, which is shown in Fig 7. The output waveform is approximately equal to sine wave and the voltage stresses on switches decreases in this topology. Stresses for H bridge inverter switches and for the central two switches of PUC, inverter is Vdc. The voltage stresses for the switches (Q1, Q2, Q5, Q6) of PUC inverter is VDC/2.

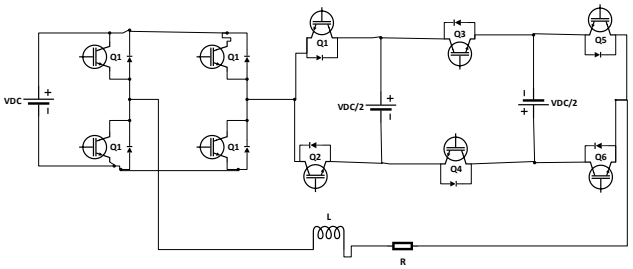


Fig 5 proposed HMLI multi-level inverter topology

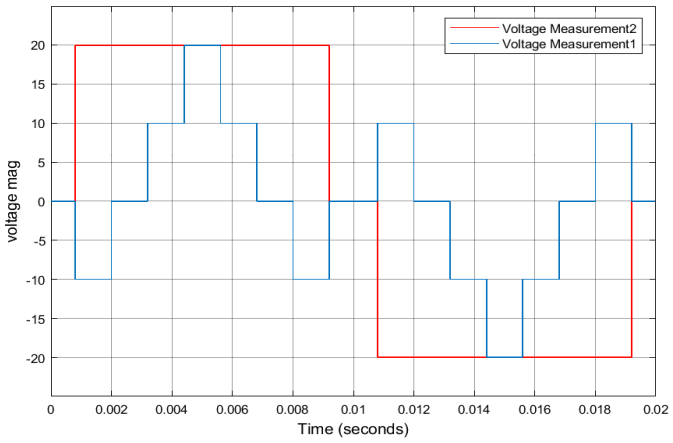


Fig 6 Combine waveform plot for H-bridge and PUC inverter

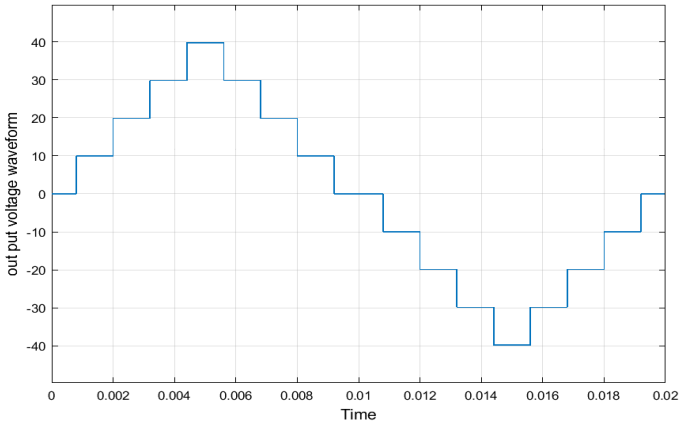


Fig 7 waveform plot for Hybrid multi-level inverter

III MATHEMATICAL EQUATIONS

The output voltage of the HMLI inverter can be obtained using equation (1):

$$V_{(HMLI)} = V_{(AB)} + V_{(BC)} \quad (1)$$

The mathematical model for the proposed HMLI converter can be represented by the following set of equations. (2)–(4):

$$di/dt = 1/L(SxVc1 + SyVc2 \pm SzVdc) \quad (2)$$

$$dvc1/dt = Sxi/C1 \quad (3)$$

$$dvc2/dt = Syi/C2 \quad (4)$$

The proposed HMLI converter can be mathematically modeled using the following set of equations. (5)–(7):

$$S_x = Q_1Q_4 - Q_2Q_3 \quad (5)$$

$$S_y = Q_4Q_5 - Q_3Q_6 \quad (6)$$

$$S_z = Q_aQ_d - Q_bQ_c \quad (7)$$

H-bridge inverter generate three level inverter while the PUC generate five level output. So the combination of two inverter generate 9 level output.

IV Circuit modes and output voltages

Mode I Vo= + Vdc/2

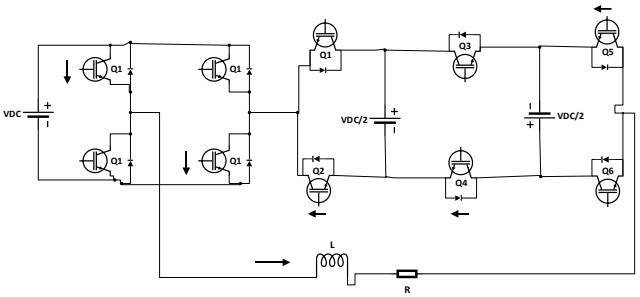


Fig 1.8 (a).

Mode II Vo= + Vdc

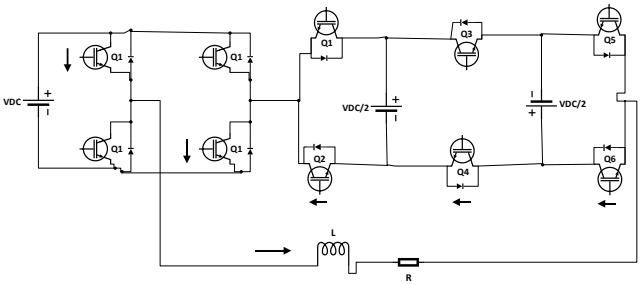


Fig 1.8 (b).

Mode III Vo= +3/2 Vdc

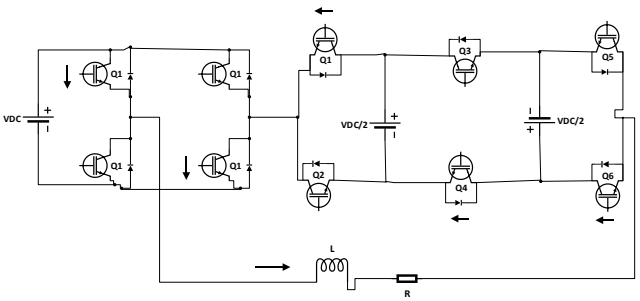


Fig 1.8 (c).

Mode IV Vo= + 2Vdc

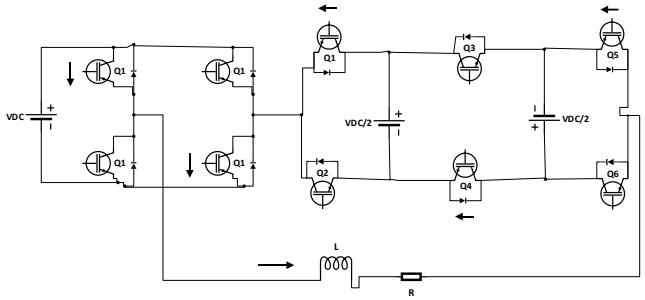


Fig 1.8 (d).

Mode V Vo= + 0 Vdc

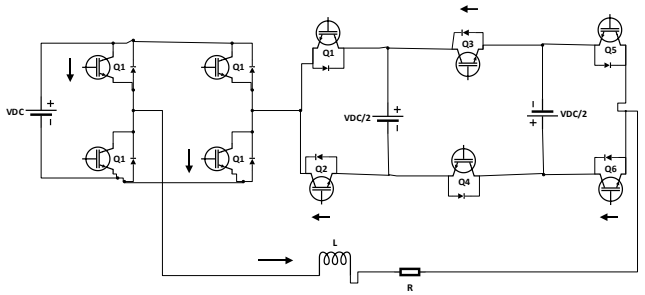


Fig 1.8 (e).

Mode VI Vo= -Vdc/2

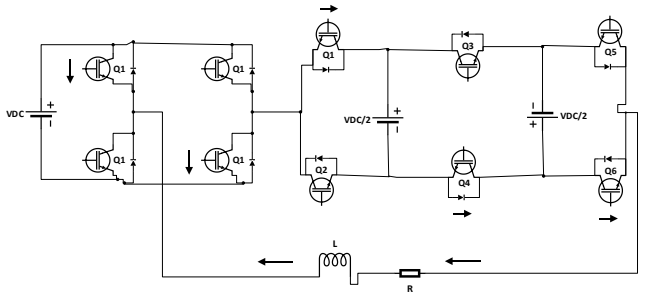


Fig 1.8 (f).

Mode VII Vo= -Vdc

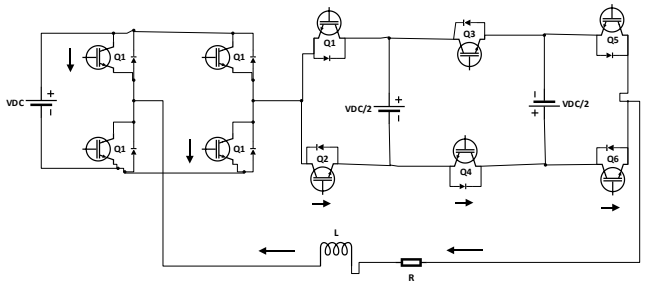


Fig 1.8 (g).

Mode VIII Vo= - 3/2Vdc

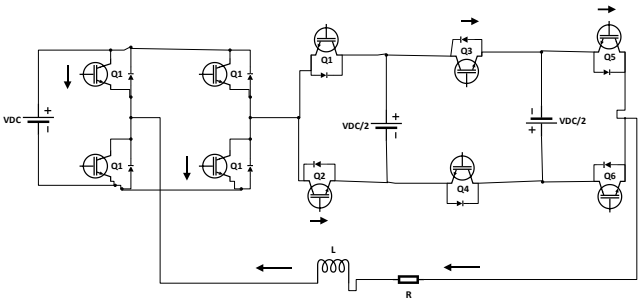


Fig 1.8 (h).

Mode IX Vo= -2Vdc

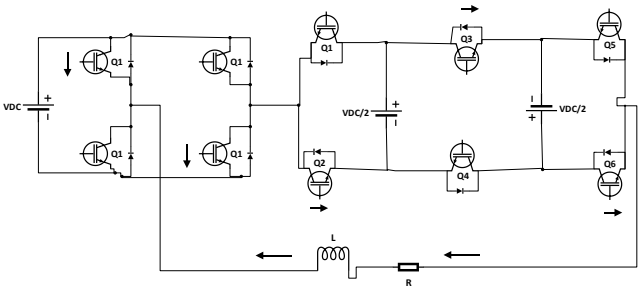


Fig 1.8 (i).

VI Modulation technique

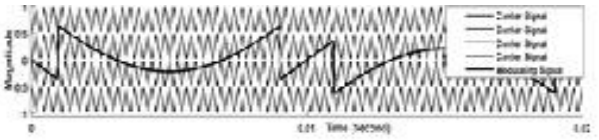
The H-bridge inverter topology employs a straightforward approach of sinusoidal Pulse Width Modulation (PWM) to minimize switching losses and decrease source Total Harmonic Distortion (THD). To generate this carrier-based PWM, multiple carrier signals are employed. The modulation technique utilized in this PWM is governed by the parameter 'm-1', where 'm' denotes the desired number of levels. Consequently, in an 'm'-level inverter, 'm-1' carrier signals are employed. In the case of a three-level H-bridge inverter, two carrier signals with a frequency denoted as fc are utilized. The Modulation index ma is determined by comparing the carrier signal frequency fc to the reference sinusoidal wave frequency fm, as described by the equation below.

$$ma = fc/fm$$

The POD carrier-based Pulse Width Modulation (PWM) technique is employed in the Packed U-Cell (PUC) configuration to generate the necessary gating signal for the six semiconductor power switches. In this PWM approach, this is based on the POD principle,

the carriers above and below the zero reference line share the same amplitude and frequency. However, carriers below the zero reference line are 180 degrees out of phase compared to the carriers above.

The PWM waveform for the PUC module utilizing the POD carrier-based technique is illustrated in Figure below.



V : Results and simulation:

The proposed HMLI inverter topology, as depicted in Figure 5, was simulated using the MATLAB/Simulink framework to assess its overall system effectiveness and performance. The simulation utilized the system parameters outlined in Table 3

Table 3: Inverter System Parameter

.

Parameter	Values
Voltage of DC Bus	50V
Carrier Freq of H Bridge	50 Hz
Voltage of DC Bus	25V
Carrier freq of PUC	5KHz
Load	R= 20 ohm L=8mH

Within the HMLI inverter model, a H-bridge inverter is interconnected in series with a 5-level Packed U-Cell (PUC) to generate a nine-level output voltage, as illustrated in Figure 7. This specific HMLI design caters to medium voltage high power applications, boasting an anticipated efficiency exceeding 98%. The selection of component values underwent meticulous scrutiny through rigorous simulations.

Figure 4 presents the simulation results of the HMLI output voltages. Figure 4(a) exhibits the H-bridge cell output voltage, Figure 4(b) displays the Packed U-Cell (PUC) output voltage, and Figure 7 depicts the HMLI output voltage.

Figures 9(c) present results of simulations of nine-level output voltage of inverter at various index modulations of Ma = 0.7, 0.8, 0.9 and 1 respectively. Specifically, Figures 9 (a, b) illustrates the results of simulations of inverter, rather than that Figure 9(c) showcases the wave form of overall output. To achieve Nine-Level output, the operations of inverter with angle three with each cycle of quarter. With ma equals to one the H-Bridge inverter transfers active power but with high harmonics generations. This type of high harmonics is subsequently controlled and compensated with help of Pack- U Cell inverter topology, resulting in a combined output waveform with nine levels.

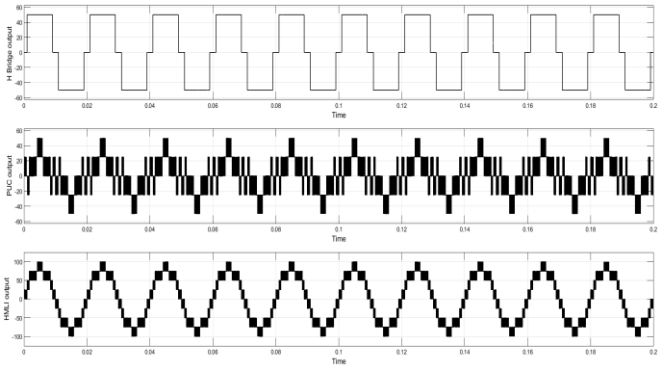


Fig 9 Nine –level hybrid multi-level inverter

(a) H-bridge output voltage (b) PUC output voltage

(c) Hybrid MLI output voltage

Figure 10 show cases the THD analysis for HMLI output for different modulation index, specifically at ma=1. In Figure 5 the circuit depicted is having simulation under ma=1 condition, the THD values are calculated for V(ab), V(bo) and the output V(ao) for HMLI inverter overall.

At ma=1, the module of PUC plays a crucial role in mitigating harmonic distortion by filtering out the 1st-order harmonic component, resulting in a nine-level output waveform. This filtering effect helps to minimize harmonics output voltage, contributing to improved waveform quality and reduced THD.

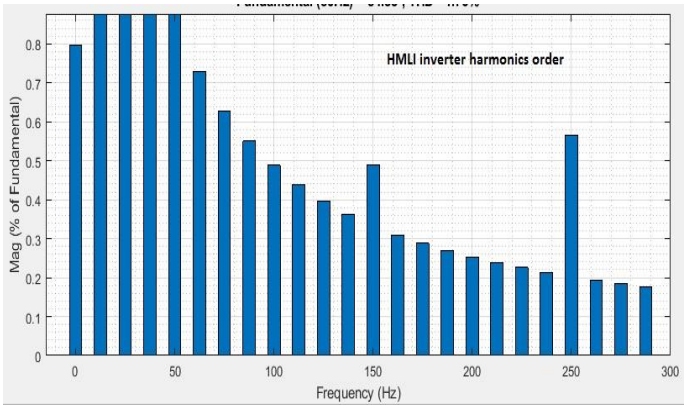


Fig 11THD harmonics order

Meanwhile, Figures 12(a) highlights the current waveforms corresponding to these modulation indexes. Additionally, Figures 12(b) provided below present the current total harmonic distortion (THD) for these modulation indexes. The total harmonic distortion (THD) for modulation index ma =1 is 1.58, which is show in fig 12.

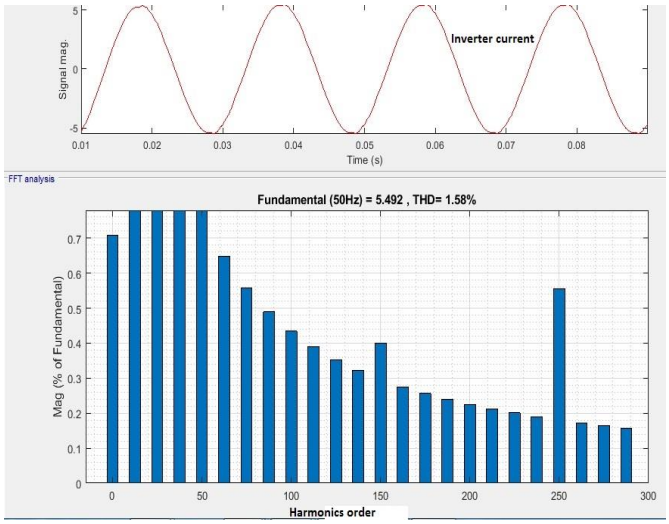


Fig 12 (a) current waveform (b) Current THD

In Figure 12(a) the current at output of inverter across the RL load for various modulation index is illustrated. By adjusting the modulation indexes while keeping the load constant, the current shows an increase. Comparing the current waveform with the inverter output, that is observed that the current lags behind the voltage waveform of the inverter. This phenomenon is attributed to inductor characteristic, wherein current lags behind voltage across the inductor.

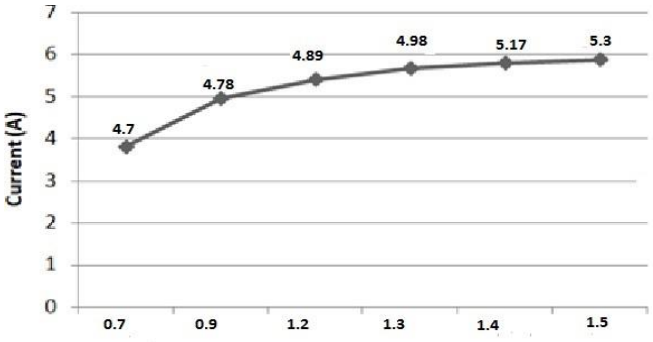


Fig 13 Modulation index

VII Comparative Analysis:

The proposed HMLI topology for the designed inverter structure aims to cater to a decrease medium voltage range of over five kV, supplying a most output voltage of nine levels. In evaluation to preceding hybrid inverter topologies with the same machine parameter mentioned in table 4 , the HMLI to topology affords numerous advantages. These inc lude a reduced switching count number, as shown in table 4, as well as a wide variety of operation and occasional cutting-edge overall harmonic distortion (THD), as indicated in table 5. These blessings set it other than the hybrid inverter topologies defined in table 5.

To limit switching losses, the highly confused switch is activated at a low switching frequency inside the HMLI topology. Consequently, the inverter's switching loss is minimized, ensuing in advanced performance as compared to the NPC VSC, as depicted. Primarily based at the inverter parameters. However, it ought to be referred to that the NPC inverter exhibits decrease current THD as compared to the AHMMC inverter. Similarly details regarding the Consequences of voltage stress on semiconductor switches are provided in table 5.

Table.4:- Components count of different inverters Inverter Components count

inverter	Active switch	Diode	Dc-link capacitor
NPC	8	4	2
HNPC with H-Bridge	10	2	3
HNPC with cascaded module	12	2	4
Proposed HMLI inverter	10	-	-

Table.5:- voltage stress on semiconductor devices

Semiconductor deice	Voltage Stress	
	Active Switches	Diode
Half bridge NPC	E/2	E/2
Half bridge	E/2	-
PUC module center cell	E	-
PUC module outer cell	E/2	-
H-Bridge	E	-

TheHMLI design utilizes four energetic switches positioned within the outer leg of the PUC module, which experience low voltage strain. As a result, those switches operate at high frequencies to decrease modern-day ripple and reduce the desired inductor size. The current overall harmonic distortion (THD) of the inverter, at distinct energy scores, is presented in table 1.5.

The desk virtually shows that the HMLI well-known shows decrease modern day THD compared to present hybrid inverter topologies.

Table.6:- Current THD of inverter operating at various power rating.

Inverter	Power rating		
	25 %	50%	100 %
NPC	5.31	2.83	1.38
HNPC with H-Bridge	6.71	3.43	1.73
HNPC with cascaded module	6.59	3.39	1.71
Proposed HMLI	6.57	3.35	1.69

Conclusion:-

The HMLI topology, designed especially for medium voltage range business programs, has been subjected to simulations at numerous modulation index values. The results exhibit that the HMLI topology generates a most nine-level output voltage with decreased voltage harmonic distortion and decrease contemporary general harmonic distortion (THD) according with the IEEE (519) requirements. Further, the HMLI topology boasts a decrease thing count in comparison to both NPC and applicable hybrid inverter topologies, whilst keeping higher performance.

Lately, multilevel inverters have received sizable traction in various industries because of high-quality advancements in their designs and manipulate strategies. The reducing value of semiconductor energy switches has made these inverters feasible for medium voltage excessive energy packages, addressing the developing strength needs of global power systems.

Widespread research has explored unique multilevel inverter topologies, reading their blessings and downsides. CHB and NPC have distinguished themselves as the topologies that are most frequently diagnosed and used in the sector. But because of their special design, multilevel inverters require a lot of switching pulses, which increases their complexity and makes it difficult to create switching approaches that would produce the appropriate trigger signals for the switches in the desired grouping. Methods like PWM and SVM were created as conventional switching algorithms. However, using separate DC elements in maximum inverter architectures poses difficulties in reducing manufacturing costs as it would necessitate a few DC capacitors with suitable voltage controls and a smaller number of DC elements.

Furthermore, this studies contributes to the improvement of multilevel rectifier topologies primarily based on the studied inverter topologies, which make use of DC capacitors to provide energetic energy to DC loads.

In short, this paper studies an innovative topology for medium voltage, high strength commercial applications, such as marble manufacturers and electric traction systems, known as an asymmetrical hybrid cascaded multilevel inverter. In a chain arrangement, this hybrid architecture

combines a H-Bridge design with a 5-degree Packed U-mobile inverter structure. This suggested hybrid architecture decreases switching losses across the H-Bridge cell and correctly mitigates harmonic contents in the IEEE (519) standards by doing away without the need for a large, bulky transformer and lowering the number of electrical components. In addition, using a POD-based fully PWM modulation methodology, low-order harmonics on the dense U-mobile module are eliminated while still maintaining a low frequency of switch for extremely low switches. The asymmetrical hybrid MLI topology enhances the electricity factor and decreases harmonic content inside the limits unique by way of IEEE requirements. The proposed inverter achieves maximum voltage levels employing the same variety of lively energy switches at different modulation indexes by adopting a modular modulation strategy.

The main finding of this study is that the suggested inverter has many advantages over similar topologies, including lower factor counts, fewer switching losses, and improved overall performance.

The suggested HMLI topology is compared to NPC in terms of issue dependability and effectiveness. The proposed inverter outperforms the NPC multilayer inverter, achieving a performance of ninety-five percent, exceeding NPC's ninety-nine percent efficiency at completely energy rating. Moreover, the suggested topology produces a nine-stage output voltage by utilizing two additional energetic switches, ensuing in greater inverter gadget performance.

FUTURE WORK

This examine has located extensive emphasis on the HMLI inverter topology, highlighting its capability benefits compared to previously suggested ones. The following guidelines define capability instructions for destiny studies, representing an initial step that could cause years of sizeable research. Building upon the machine's design and modeling, the subsequent section involves constructing a small-scale prototype of the HMLI. This prototype targets to validate and improve upon the effects obtained from the theoretical have a look at.

Inside the proposed HMLI topology, the DC voltage assets inside the low voltage cellular can be substituted with capacitors, and an evaluation of the machine's overall performance will be performed consequently. A controller might also be developed to maintain balanced DC hyperlink capacitor voltage. For the voltage balancing and DC hyperlink voltage-tampering module, an analytical technique may be investigated.

Through the conversion of one in every DC source of the inverter, the equivalent recommended HMLI topology can produce an output voltage of 11 levels. This could also improve the HMLI’s typical efficiency and lower THD. The proposed analysis can eventually be expanded to a three-phase device configuration, allowing for the investigation of novel modulation as well as control strategies for this particular device.

These future endeavors will contribute to deeper information of the HMLI topology, its sensible implementation, and the improvement of advanced modulation and control strategies for more suitable system performance.

III. REFERENCES

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