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Improved Control Method for Voltage Regulation and Harmonic Mitigation Using Dynamic Voltage Restorer

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Abstract – The increasing concerns of sensitive industrial customers and electrical utility corporations regarding Power Quality (PQ) issues have driven the development of innovative solutions. This paper introduces an enhanced control method based on Smooth Approximation Super Twisting Algorithm (SASTA) for the Dynamic Voltage Restorer (DVR) to achieve effective regulation of the critical load (CL) voltage to its nominal value while compensating for harmonics induced by the grid. The findings highlight the significance of the improved control method in enhancing the DVR's performance for voltage regulation and harmonic distortion compensation. By implementing this control system, the DVR successfully mitigates deviations in voltage amplitude and reduces harmonic distortions in the CL voltage, thereby improving power quality. To evaluate the performance of the proposed control method, extensive simulations are conducted using the MATLAB/Simulink SimPower System toolbox. The results demonstrate that the SAST-SMC for the DVR can accurately regulate the voltage in less than 2.3 milliseconds (ms) and harmonics mitigation under 5% as per IEEE standards.

Keywords – Dynamic Voltage Restorer, Power Quality Improvement, Sliding Mode Control, Harmonics Mitigation, Voltage Regulation, Smooth Approximation Super Twisting Algorithm

I. INTRODUCTION

In this electrified world, the electrical power companies are concentrating on the uninterruptible high-quality power delivery to the end energy user due to meet the soaring energy demand and contest among private energy supplier companies [1]. Since the electrical power system is highly dynamic in nature, the electrical load is varying all the time hence electrical parameters fluctuate [2]. In general, any variation or problem in electrical parameters such as voltage, frequency, phase angle, or current that leads to failure/malfunction in the system is considered as power quality (PQ) issues [3]. Among PQ issues, voltage regulation is the frequently occurring problem (VR) [4]. VR causes' substantial financial loss to industrial customers by reducing the voltage levels from normal operating voltages of electrical machines.

However, the VR severity is not as problematic issue as its occurring frequency in the power system. The VR causes issues at energy user ends and sensitive industrial loads. VR may result in the tripping of devices, data loss, and failure of equipment [5].

As per IEEE standards, VR refers to the control and maintenance of voltage levels within specified limits in an electrical power system. IEEE (Institute of Electrical and Electronics Engineers) has established several standards that outline the acceptable voltage ranges and the permissible deviations from the nominal voltage level [6].

The IEEE standard for voltage regulation varies depending on the application and the specific power system. In general, IEEE 519-2014, titled "IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems," provides guidelines for voltage regulation in electrical power systems to mitigate harmonic distortions and maintain power quality [7].

According to IEEE 519-2014, the recommended voltage regulation limits for power systems are typically defined in terms of the percentage deviation from the nominal voltage level. For example, the standard may specify a voltage regulation limit of ±5% or ±10% of the nominal voltage level [7].

Voltage regulation standards are important to ensure the stable operation of electrical equipment and to avoid potential issues caused by voltage fluctuations. Compliance with these standards helps prevent damage to sensitive equipment, minimize power quality problems, and maintain a reliable and efficient power supply.

Similarly, Harmonics, as per IEEE standards, refer to the undesirable distortion of the electrical waveform in a power system caused by non-linear loads. IEEE has established standards to mitigate harmonics and maintain acceptable levels of harmonic distortion in electrical power systems.

The IEEE standard that specifically addresses harmonics is IEEE 519-2014, titled "IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems." This standard provides guidelines and requirements for limiting harmonic distortion levels in power systems [7].

According to IEEE 519-2014, the standard defines Total Harmonic Distortion (THD) as the measure of harmonic distortion in a power system. THD represents the percentage of the root mean square (RMS) value of the harmonics to the RMS value of the fundamental frequency component.

The standard recommends limits for THD depending on the type of power system and the location of the harmonic sources. The limits are typically expressed as a percentage of THD. For example, in distribution systems, the standard suggests maintaining THD below 5% for voltage distortion and below 8% for current distortion.

The distribution system in a power network is the weakest part because of load connection and its dynamic nature, which may cause major faults and losses in this area. It has a shallow voltage profile as compared to power generation and transmission because of exposure to faults, interconnected/radial network, and varying load conditions. It has the highest X/R ratio compared to the transmission system, which results in high power loss (up to 13%) and voltage instability [8].

There are various methods to alleviate PQ problems in power systems, especially in the distribution network. The conventional methods for improving the voltage profile of the electrical power system are by using uninterruptible power supplies (UPS), capacitor banks, tap changers, and installing new feeders in parallel with existing lines. However, these methods have limitations and complete mitigation of power issues is not possible. Limitations cause the power quality issues because of their uncontrollable reactive power compensation and high equipment cost etc. Similarly, UPS takes the entire load and has no sharing option with utility. While tap changer has bulky construction requirements [9]. Dynamic compensation devices and control methods provide a solution to these problems by incorporating renewable and backup power sources as per demand. It is also beneficial in reducing the cost and emission of the operating system [10].

In recent years, the semiconductor industries have progressed rapidly, produced precisely controllable switches, and introduced Custom power devices (CPD) in the power network. CPDs are used at the distribution levels to alleviate power quality problems such as voltage sag. Commonly used CPDs are Unified Power Quality Conditioner (UPQC), Dynamic Voltage Restorer (DVR), and Distribution Static Compensator (DSTATCOM). Among CPDs, DVR is commonly used due to its numerous advantages such as reliability, efficiency, smaller size, economics, and its dynamic response [11].

State feedback, self-tuning, instantaneous reactive power theory, and many more control methods all have advantages and disadvantages when it comes to generating a pure AC waveform at the output of voltage source converters in DVRs [12]. They are designed to produce an accurate, linearized, and useful mathematical model of the system under operational conditions. These control systems, however, are unable to provide the greatest performance as the parameters of the system change. Therefore, a trustworthy and effective control system that can function with high accuracy and stability in dynamic settings is needed. The DVR with SMC can operate very efficiently. It is not sensitive to changes in system properties and does not necessitate a comprehensive mathematical model of the system.

This paper introduces an enhanced control method based on Smooth Approximation Super Twisting Algorithm (SASTA) for the Dynamic Voltage Restorer (DVR) to achieve effective regulation of the critical load (CL) voltage to its nominal value while compensating for harmonics induced by the grid.

II. DYNAMIC VOLTAGE RESTORER STRUCTURE

The DVR consists of a DC storage source, voltage source converter (VSC), filter, boosting transformer, and most importantly a precise and accurate control strategy for switching of VSC. DVR is shown in Fig 1. DVR performance is mainly dependent upon the control strategy for switching of VSC.

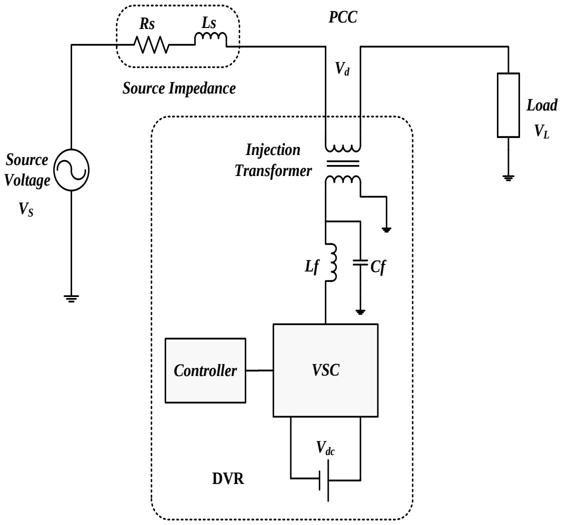


Fig 1: DVR Structure and its connection with Distribution Network

The main task of any control strategy of a DVR is the accurate and efficient detection of VR/Harmonics occurrence in the power network, calculation of the PQ issues in the network, calculation of required reactive power for injection, signaling of PWM/SPWM for switching of IGBTs of VSC (operating in inverter mode), making sure the correction of voltage issues by series injection and measurement with a closed-loop scheme, and termination of PWM/SPWM trigger pulses once the VR/Harmonics event has passed.

III. MATHEMATICAL MODELLING OF DVR

Fig 2. shows the schematic diagram of DVR connected in series with the distribution system having source and load.

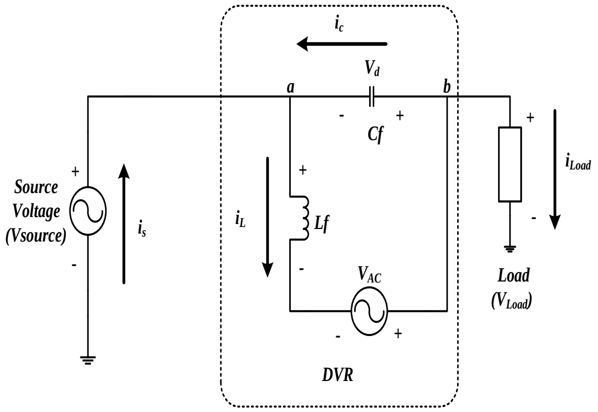


Fig 2: Schematic diagram of DVR in the distribution system

The final DVR's state space model equation is [2];

$$\frac{d}{dt}\begin{bmatrix} i_L \\ V_d \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_f} \\ \frac{1}{C_f} & 0 \end{bmatrix}\begin{bmatrix} i_L \\ V_d \end{bmatrix} + \begin{bmatrix} 0 & \frac{1}{L_f} \\ \frac{-1}{C_f} & 0 \end{bmatrix}\begin{bmatrix} i_s \\ V_{AC} \end{bmatrix} \quad (1)$$

Where

$I_{L,}$ V_d = state variables

I_s and V_{AC} = input variables

IV. MATHEMATICAL MODELLING OF SASTA-SMC

A sliding surface to mitigate VR/Harmonics is selected such that it can control the output of VSC of DVR. The first derivative of V_d has no control on input V_{AC}. Therefore, the second derivative of V_d is computed such that:

$$\frac{dV_d}{dt} = \frac{(i_L - i_s)}{C_f} = x_1 \quad (2)$$

Derivative of equation (6);

$$\frac{dx_1}{dt} = \frac{1}{C_f}\left(\frac{(V_{AC} - V_d)}{L_f} - \frac{di_s}{dt}\right) \quad (3)$$

State space model of voltage injected by DVR changes to

$$\frac{d}{dt}\begin{bmatrix} V_d \\ x_1 \end{bmatrix} = \begin{bmatrix} x_1 \\ \frac{1}{C_f}\left(\frac{(V_{AC}-V_d)}{L_f} - \frac{di_s}{dt}\right) \end{bmatrix} \quad (4)$$

The implementation of SMC for DVR required three steps;

- Designing Sliding Manifold
- Reachability Conditions
- Determination of Control law

A. Designing Sliding Manifold

The sliding manifold is a surface or line on which the system is stable and exhibits good performance. Once the state trajectories are moved from this surface, the controller should bring the state trajectories to the origin and stay on this surface. For this purpose, the voltage difference V_{diff} is calculated by;

$$V_{diff} = V_{ref} - V_{Load} \quad (5)$$

The selection criteria for the sliding surface is the difference between V_{diff} and voltage injected by DVR, which results in equation (6), where k is feedback control gain. Fig. 3 shows the Block diagram of SAST-SMC for DVR.

$$S = V_{err} + k\frac{d}{dt}V_{err} \quad (6)$$

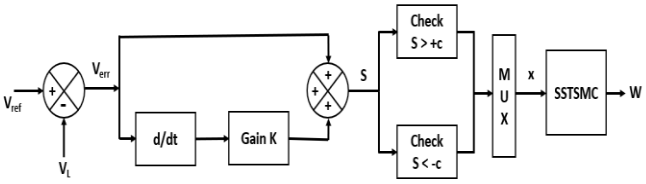


Fig. 3. Block diagram of SAST-SMC for DVR

B. Reachability Conditions

To ensure the safe operation of controller is through bringing state variables to sliding manifold, the following two conditions must be satisfied;

Condition-1: $S = 0$

Condition-2: $\dot{S} = 0$

C. Determining Control Law

The control law is formulated as shown in equation (7);

$$x(t) = \begin{cases} +1 if\ S > +\alpha \\ -1 if\ S < -\alpha \end{cases} \quad (7)$$

Where *x(t)* is the input control variable, α is constant, and the value of *x* is selected based on ±*α*. When the value of *x (t) = +1*, the Switch-1 and Switch-2 are on. Similarly, when the value of *x (t) = -1*, the Switch-3 and Switch-4 are on. The smooth super twisting algorithm is employed to implement practically and to remove chattering. The switching rule applies the Smooth Super Twisting Algorithm (SSTA) to the sliding manifold to deliver the updated input of control "U" as indicated in (8) [1]:

$$U = n_1 + n_2 = -[(k_1 sat(S)\sqrt{|S|}) + (k_2 \int (sat(S)ds))] \quad (8)$$

V. DESCRIPTION OF TEST SYSTEM

Fig 4. shows the proposed test system configuration to carry out the transient modeling and simulation of the DVR with the associated control strategies. The total simulation period is 0.30 seconds. The distribution model includes 400V, 50 Hz supply system with 1.57Ω source resistance and 15.70 mH source inductance, three-phase linear load with 10 kW active power (P) and 1 kvar reactive power (Q), a three-phase 10kVA injection transformer (40-400V) is used to connect the DVR of 40V DC energy storage with 55mF capacitance and 1.8mH inductive filter to the distribution system and its associated control techniques.

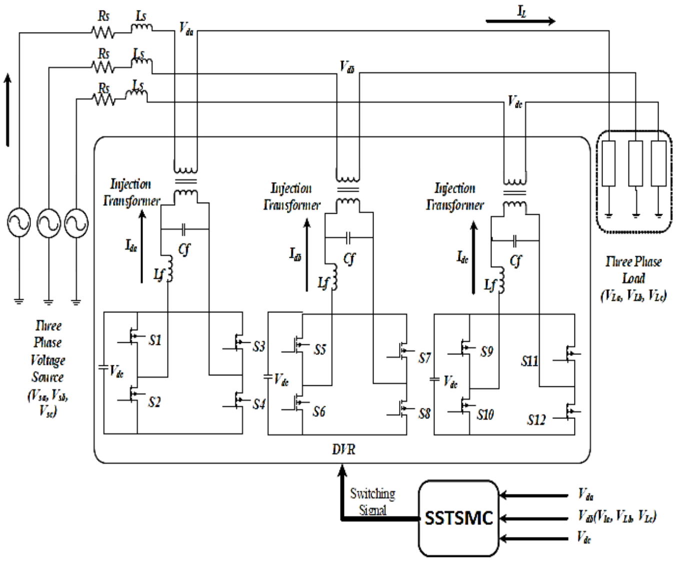


Fig 4: DVR is connected with Distribution system

The analysis that follows evaluates how well the suggested control approach performed.

- Voltage Regulation
- Harmonics Mitigation

The SSTSMC does not provide a signal to the DVR to operate when there is no fault with the system voltage (normal state). When the system voltage varies outside of the permitted range, the controller begins to function. SSTSMC functions as follows:

i. Check for voltage spikes or dips.
ii. Determine the voltage peaks and troughs (in percentage).
iii. Ascertain the signal used to regulate switching.
iv. Produce the switching signal for voltage source converters using pulse width modulation.
v. Create the necessary switching signal continuously to make sure voltage faults are corrected.
vi. Stop the switching of converters once the fault has been corrected.

VI. RESULTS

A three-phase programmable voltage source produces a 30% balanced voltage dip from 0.1 seconds to 0.2 seconds. At the period t= 0.1 sec to 0.2 sec, a voltage source inverter-based DVR is connected to a distribution system and injects a compensation voltage to regulate the voltage across critical load and mitigate voltage harmonics.

Fig 5 shows the RMS Voltage waveform of source voltage under-voltage sag of 30%. At 0.1 sec, the SSTA-SMC-based controller detects the disturbance in the voltage and injects the desire compensation voltage with proper magnitude of almost 1 p. u. into the distribution system, as shown in fig 5. This controller mitigates the VR in 2.3 ms which is less than the tolerable limit of less than 20 ms according to SEMI F-47 standard and IEEE standard for sensitive loads.

The total harmonic distortion (THD) value of all phases of uncompensated and compensated voltage are shown in Fig 6 (a-f) which is lower than the tolerable limit of 5% according to IEEE std. 1159-1995 and SEMI F-47 standard for sensitive loads.

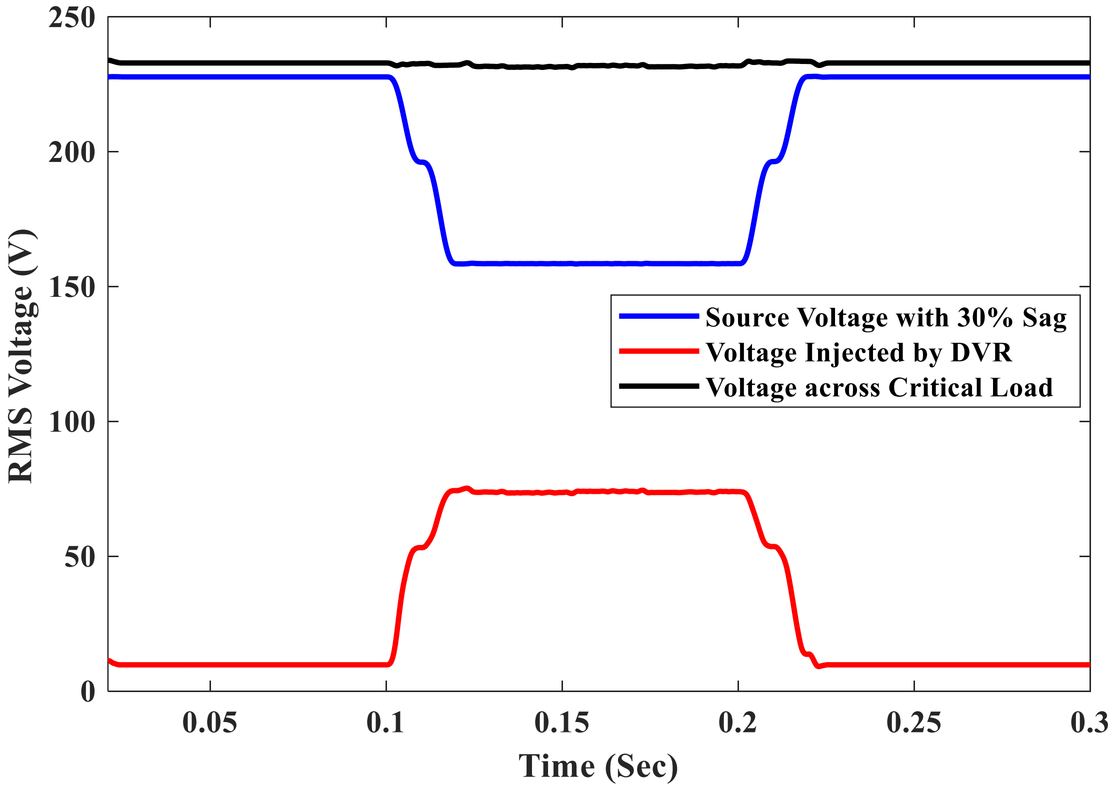
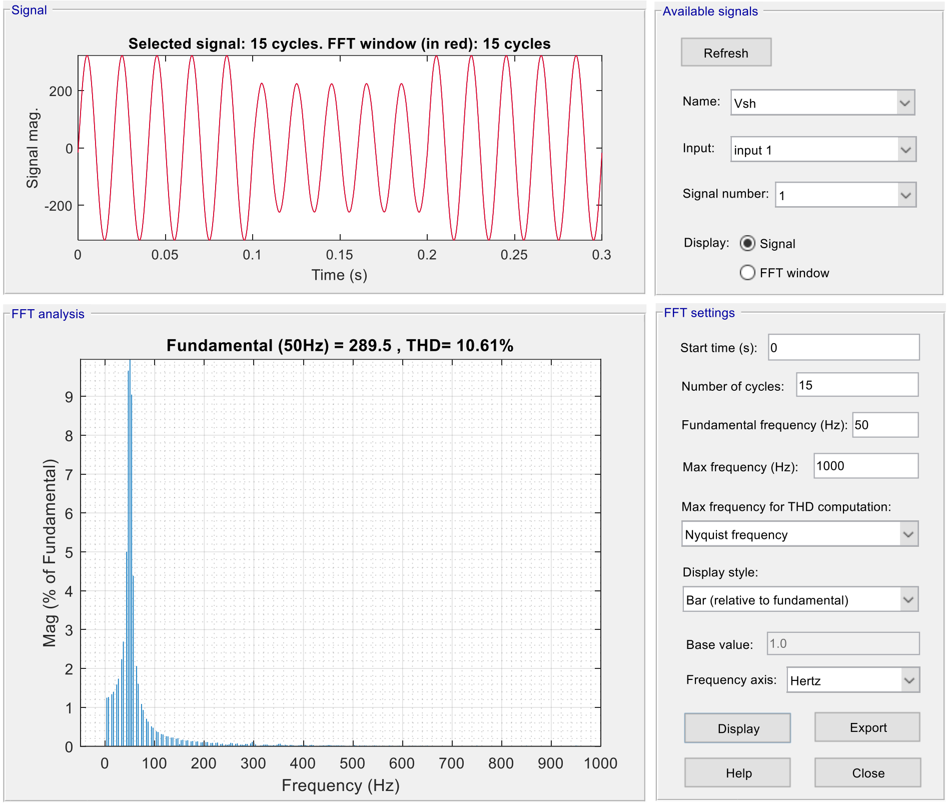


Fig 5. RMS Voltage Waveforms of Source Voltage, DVR Injected Voltage, and Critical Load Voltage



Name: Vsh

Input: input 1

Signal number: 1

Display: ● Signal ○ FFT window

Start time (s): 0

Number of cycles: 15

Fundamental frequency (Hz): 50

Max frequency (Hz): 1000

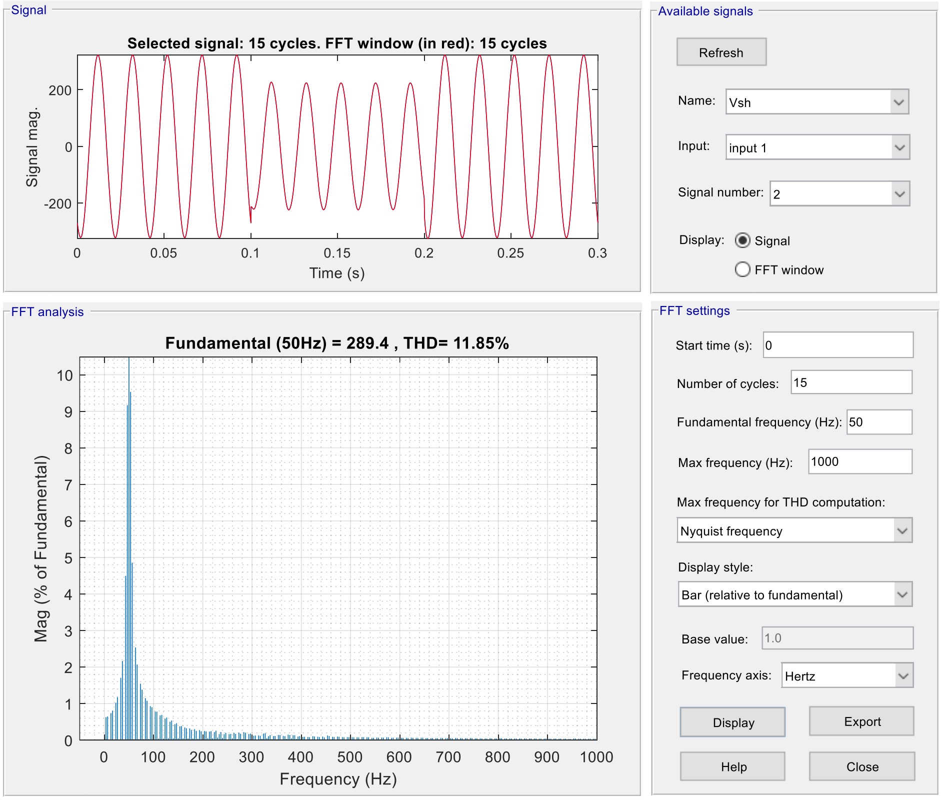
Max frequency for THD computation: Nyquist frequency

Display style: Bar (relative to fundamental)

Base value: 1.0

Frequency axis: Hertz

Fig 6(a). THD of Uncompensated Voltage (Phase A)



Name: Vsh

Input: input 1

Signal number: 2

Display: ● Signal ○ FFT window

Start time (s): 0

Number of cycles: 15

Fundamental frequency (Hz): 50

Max frequency (Hz): 1000

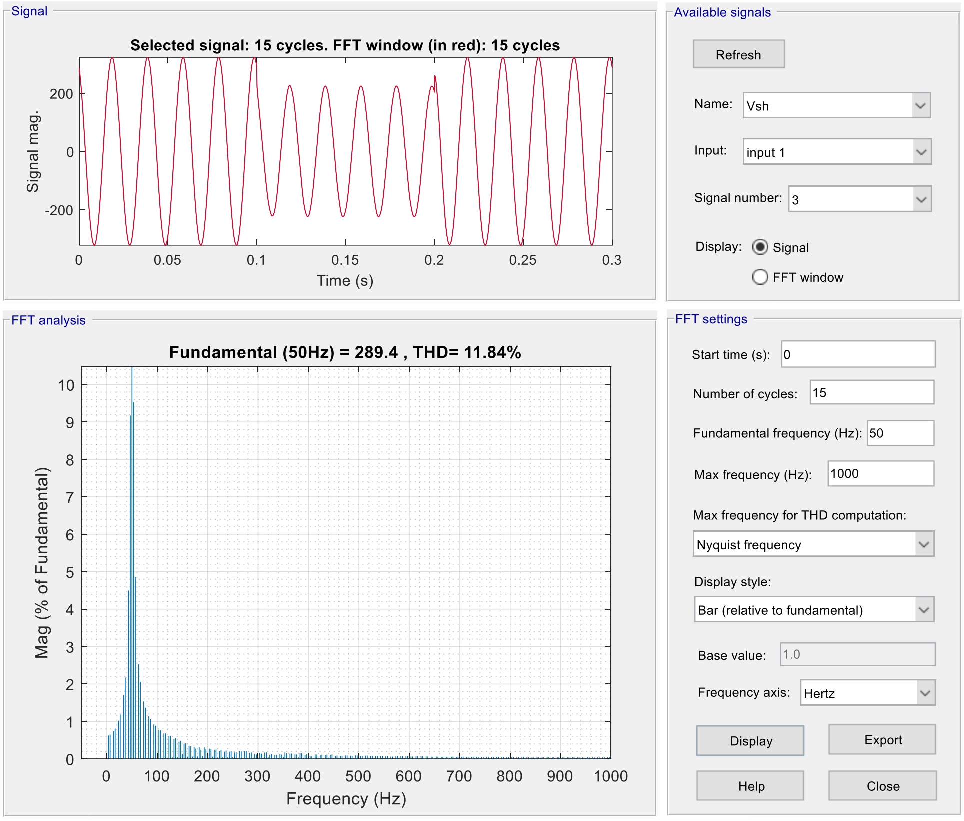
Max frequency for THD computation: Nyquist frequency

Display style: Bar (relative to fundamental)

Base value: 1.0

Frequency axis: Hertz

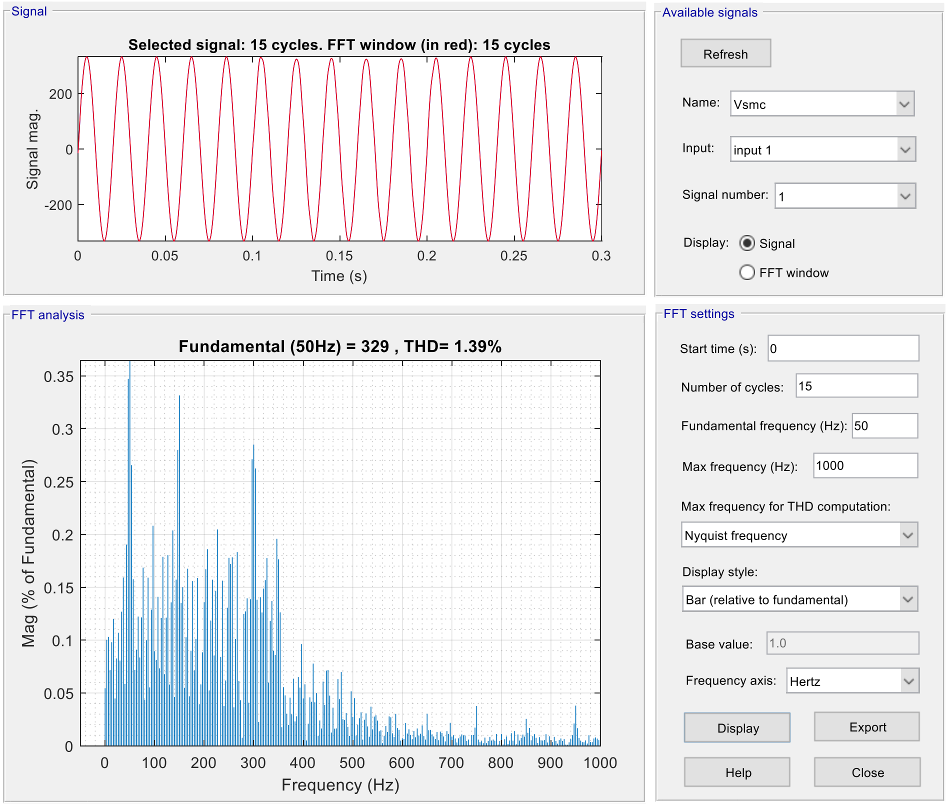
Fig 6(b). THD of Uncompensated Voltage (Phase B)



Name: Vsh
Input: input 1
Signal number: 3
Display: ● Signal ○ FFT window

Start time (s): 0
Number of cycles: 15
Fundamental frequency (Hz): 50
Max frequency (Hz): 1000
Max frequency for THD computation: Nyquist frequency
Display style: Bar (relative to fundamental)
Base value: 1.0
Frequency axis: Hertz

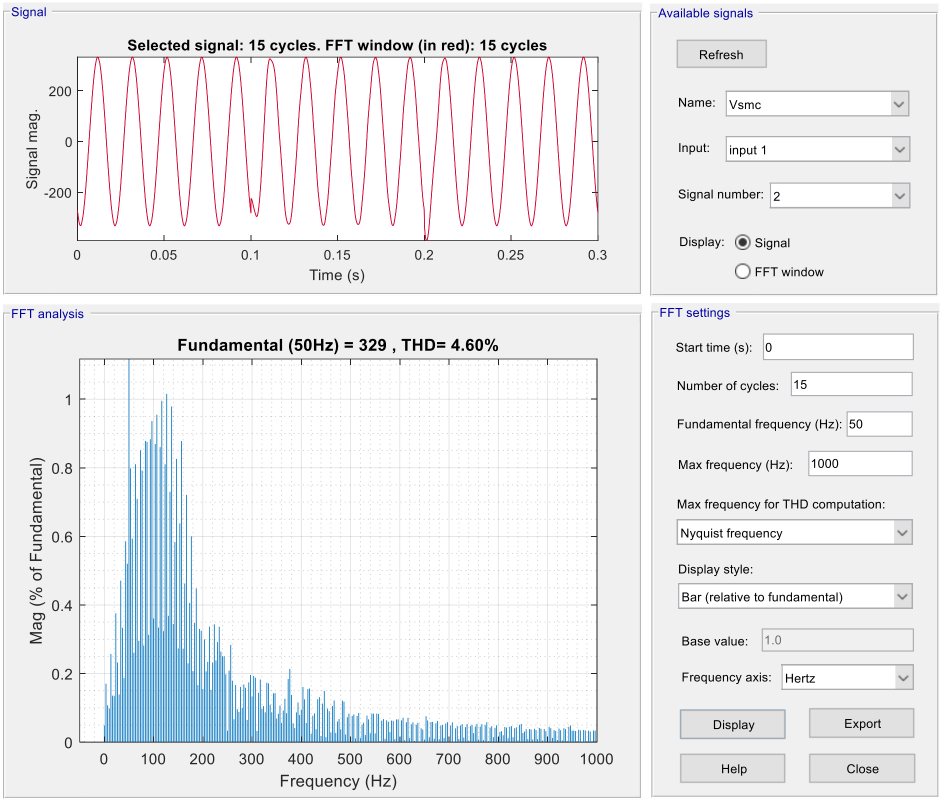
Fig 6(c). THD of Uncompensated Voltage (Phase C)



Name: Vsmc
Input: input 1
Signal number: 1
Display: ● Signal ○ FFT window

Start time (s): 0
Number of cycles: 15
Fundamental frequency (Hz): 50
Max frequency (Hz): 1000
Max frequency for THD computation: Nyquist frequency
Display style: Bar (relative to fundamental)
Base value: 1.0
Frequency axis: Hertz

Fig 6(d). THD of Compensated Voltage (Phase A)



Name: Vsmc

Input: input 1

Signal number: 2

Display: ● Signal ○ FFT window

Start time (s): 0

Number of cycles: 15

Fundamental frequency (Hz): 50

Max frequency (Hz): 1000

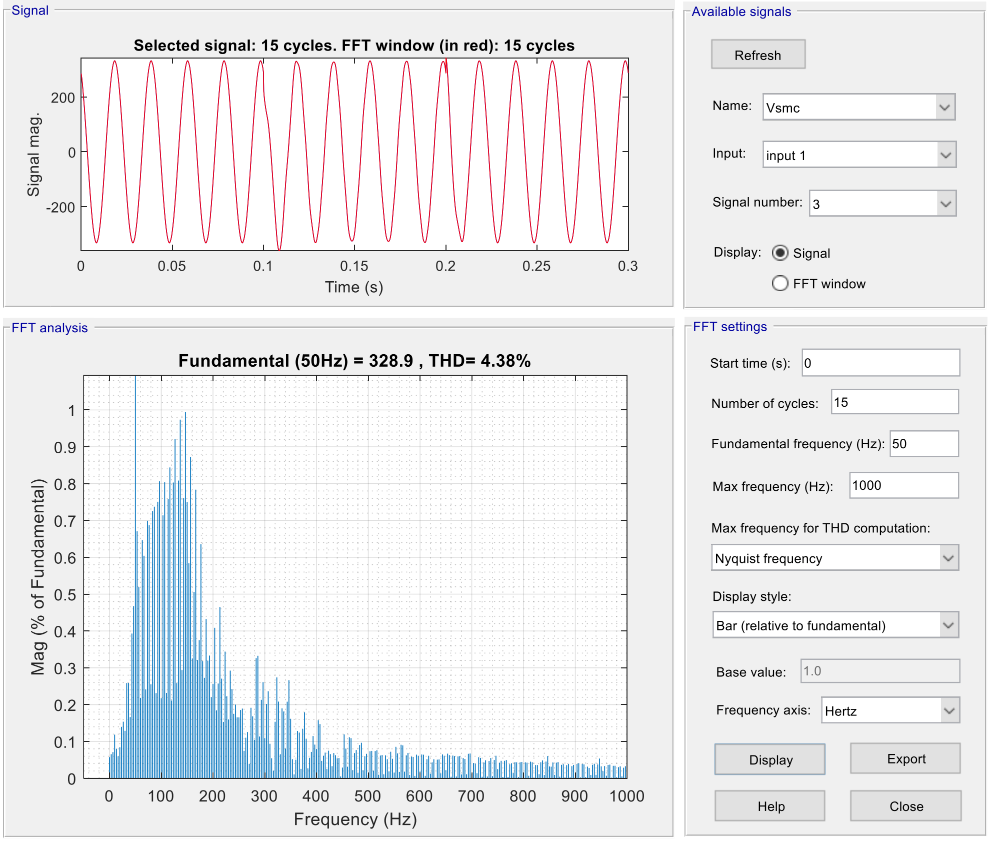
Max frequency for THD computation: Nyquist frequency

Display style: Bar (relative to fundamental)

Base value: 1.0

Frequency axis: Hertz

Fig 6(e). THD of Compensated Voltage (Phase B)



Name: Vsmc

Input: input 1

Signal number: 3

Display: ● Signal ○ FFT window

Start time (s): 0

Number of cycles: 15

Fundamental frequency (Hz): 50

Max frequency (Hz): 1000

Max frequency for THD computation: Nyquist frequency

Display style: Bar (relative to fundamental)

Base value: 1.0

Frequency axis: Hertz

Fig 6(f). THD of Compensated Voltage (Phase C)

VII. **CONCLUSION**

The growing concerns of both sensitive industrial customers and electrical utility corporations regarding Power Quality (PQ) issues have spurred the development of innovative solutions. This research paper introduces an advanced control method utilizing the Smooth Approximation Super Twisting Algorithm (SASTA) for the Dynamic Voltage Restorer (DVR). The primary objective is to effectively regulate the voltage of the critical load (CL) to its nominal value while compensating for grid-induced harmonics. The results obtained from this study underscore the importance of the improved control method in enhancing the performance of the DVR concerning voltage regulation and harmonic distortion compensation. By implementing this control system, the DVR effectively mitigates deviations in voltage amplitude and reduces harmonic distortions in the CL voltage, thus leading to an overall improvement in power quality. To evaluate the effectiveness of the proposed control method, extensive simulations were conducted using the MATLAB/Simulink SimPower System toolbox. The simulation results clearly demonstrate that the SAST-SMC for the DVR achieves accurate voltage regulation within a response time of less than 2.3 milliseconds (ms) while effectively mitigating harmonics to levels below 5%, in accordance with the standards set by IEEE. These findings highlight the significant contributions of the SASTA-based control method in enhancing the performance of DVRs. The proposed approach successfully addresses voltage regulation and harmonic distortion compensation, leading to improved power quality. The extensive simulations conducted using MATLAB/Simulink validate the efficacy of the control method, showcasing its ability to regulate voltage and mitigate harmonics within the specified time limits and according to IEEE standards. In conclusion, the integration of the Smooth Approximation Super Twisting Algorithm (SASTA) into the control system of the Dynamic Voltage Restorer (DVR) proves to be a valuable solution for enhancing power quality. The proposed control method effectively regulates the critical load voltage and compensates for grid-induced harmonics, thereby mitigating voltage deviations and reducing harmonic distortions. The outcomes of extensive simulations support the effectiveness of the SASTA-based control method in achieving the desired objectives, improving power quality, and meeting the requirements set by IEEE standards.

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