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FPGA Implementation of 5-level Neutral Point Clamp Inverter

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Abstract – Since multilevel inverters have complex switching schemes, it is an important requirement to generate fast and easy switching signals. FPGA has the feature of fast and parallel operation and has been widely used in the field of power electronics in recent years. In this study, a fast signal generation of Sinusoidal Pulse Width Modulation (SPWM) technique using Field Programmable Gate Array (FPGA) for 5-level single-phase Neutral Point Multilevel Inverter (NPC-MLI) is described. In the study, the analysis and simulation of the NPC-MLI topology was carried out in the MATLAB/Simulink environment. The control algorithm for the switching components in the NPC-MLI topology is created with XSG block sets in the MATLAB/Simulink environment. The SPWM technique, which is common in literature, was used as the control algorithm and the basic principles of the SPWM technique were mentioned in detail. In the experimental study, the control algorithm created in the MATLAB/Simulink environment was automatically converted to HDL code, run in VIVADO software and embedded in the FPGA environment. Both simulation and experimental measurements of the signals used to drive the switching components in the NPC-MLI topology are shown. In the simulation study, a load is connected to the output voltage of the NPC-MLI topology and analyzed both with filter and without filter. While the Total Harmonic Distortion (THD) value was 27.06% without filter, it was observed that the THD value was 1.24% with filter. As a result of the simulation and experimental studies, it has been seen that the SPWM method has been successfully implemented in the FPGA environment for the 5-level single-phase NPC-MLI topology. In conclusion, this study shows that the FPGA-based SPWM method can be used effectively for the generation of fast switching signals of multilevel inverters, which is an important application in the field of power electronics.

Keywords – Multilevel Inverters (MLI), Neutral Point Multilevel Inverters (NPC-MLI), SPWM, FPGA, XSG

I. INTRODUCTION

Multilevel inverters (MLI) play an important role in today's industrial applications as DC-AC converters, both in terms of convenience and solution. MLIs are used in power system applications such as renewable energy, High Voltage DC (HVDC). It is also common in power quality devices such as flexible AC transmission systems (FACTS), static compensators (STATCOM), motor drives, conveyors [1]. MLIs have significant advantages in terms of low Total Harmonic Distortion (THD), high power quality, low switching losses, lower dv/dt in switching components, better electromagnetic interference (EMI), high voltage capability. Thanks to these advantages, its popularity is increasing in many industrial applications [2].

There are three classical multilevel inverters that are well known in literature. These are Neutral Point Clamp (NPC), Floating Capacitor (FC) and Cascade H-Bridge (CHB) multilevel inverters. In this study, NPC-MLI topology, which is one of these classical methods, was studied [3]. NPC-MLI, also called diode clamped, has attracted

attention especially in industrial applications where power electronics have been used for the last two decades, due to its low EMI and high efficiency [4].

FPGA developed by Xilinx Inc. consists of thousands of logic gates gathered in a configurable logic block. Because the FPGA is both configurable and programmable, it is very useful for prototyping an Application Specific Integrated Circuit (ASIC). Thanks to its FPGA parallel processing feature, it can run complex control algorithms in a short time. However, the implementation of control algorithms in FPGA for real-time control applications is difficult, time consuming and requires special knowledge in terms of Hardware Description Language (HDL). In order to overcome this difficulty, thanks to XSG, HDL code embedded in the FPGA development board can be produced in the MATLAB/Simulink environment without the need for HDL knowledge. Therefore, it is easier to generate HDL code for PWM signals with XSG [5].

In this study, switching signals are generated for 5-level NPC-MLI topology using FPGA development board. After the proposed FPGA-based switching strategy and 5-level NPC-MLI topology are explained, the simulation and experimental outputs of this study are given.

II. NPC-MLI CIRCUIT TOPOLOGY

The NPC-MLI topology, which is frequently used in the literature, is also called diode clamped. In the NPC-MLI topology, first proposed in 1981, there is only one DC voltage source, while capacitors are used to divide the DC voltage source and provide the neutral point. In an N-level NPC-MLI topology, the number of capacitors is (N-1), the number of switching components connected in series is 2*(N-1), and the number of clamping diodes used to block the current is (N-1)*(N-2). Thus, by increasing the number of voltage levels, the quality of the voltage at the output of the relevant topology is improved and the voltage waveform becomes close to the sinusoidal waveform. Also, the THD of the output waveform will be lower [6, 7]. The 5-level NPC-MLI topology shown in Figure 1 consists of 8 switching elements, 12 clamping diodes, 4 capacitors and a DC voltage source. The output voltage levels of the circuit in Figure 1 are $+V_i/2$, $+V_i/4$, 0, $-V_i/2$, $-V_i/2$.

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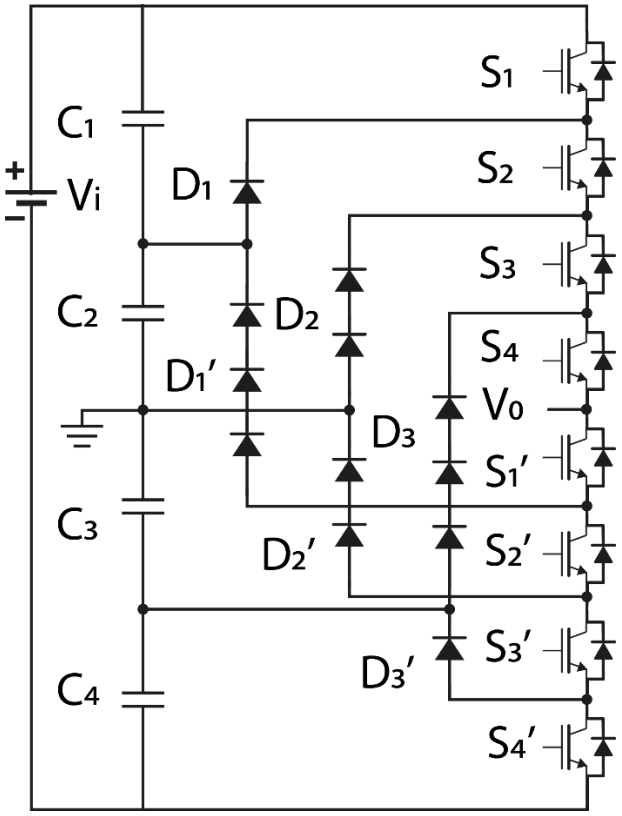

Fig. 1. 5-level NPC-MLI topology

The output voltage of the 5-level NPC-MLI topology in Figure 1 can be created using the following switching combinations:

• For V_o=0 output voltage, two upper switches S_3 and S_4 and two lower switches S_1' and S_2' become short-circuited.

• For V_o=+ V_i/4 output voltage, three upper switches S_2, S_3, and S_4 and one lower switch S_1' become short-circuited.

• For V_o=+ V_i/2 output voltage, all upper switches S_1, S_2, S_3 and S_4 are short-circuited.

• For V_o=- V_i/4 output voltage, one upper switch S_4 and three lower switches S1', S2' and S3' become short-circuited.

• For V_o=- V_i/2 output voltage, all lower switches S_1', S_2', S_3' and S_4' become short-circuited.

The state variables of the five different switching modes of the NPC-MLI topology are given in Table 1.

Table 1. Switching states and voltage levels

Vo	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$+V_i/2$	1	1	1	1	0	0	0	0
$+V_i/4$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_i/4$	0	0	0	1	1	1	1	0
$-V_i/2$	0	0	0	0	1	1	1	1

III. GENERATION OF PWM SIGNAL IN XSG

While the PWM method gives a logical "1" in a certain time interval during a period, it gives a logical "0" in the remaining time interval. The modulated f(t) square signal consists of a duty cycle (D), a high value (y_max) and a low value (y_min) [5]. The f(t) signal is mathematically defined as:

$$y = \frac{1}{T}\int_0^T f(t)dt \qquad (1)$$

When f(t) is a square wave signal, it takes the maximum value at the highest duty cycle and takes the minimum value at the low value of the duty cycle [5]. If equation (1) is rearranged:

$$f(x) = D.y_{max} + (1 - D).y_{min} \qquad (2)$$

Many controlled switching components are used to produce stair-type output in MLI topologies. The switching configuration and duration of each step play an important role in reducing THD. SPWM technique, which is widely used in power electronics inverter applications [8]. This technique has advantages such as low switching losses, ease of implementation and less harmonic output [5].

In this study, Level Shift SPWM technique, which was created using XSG simulation tools, was carried out in the FPGA environment. Triangle carrier signal and modulating sinusoidal wave signal are generated with XSG block sets in MATLAB/Simulink environment. The system created with XSG block sets is compiled and HDL code is automatically generated. The produced HDL code is run in VIVADO software and embedded in the FPGA environment.

Using the multi-carrier PWM method, the appropriate output of the switching components in MLI topologies is controlled. The working principle of SPWM is to obtain high and low state by comparing triangular carrier waves with reference sinusoidal modulating waves. If the amplitude of the carrier wave is less than the amplitude of the modulating wave, it will be the high state, otherwise it will be the low state. In the high state, the switching component turns on, while in the low state it turns off [9, 10]. In Level Shift SPWM technique, (m-1) carrier signals are used for m-level MLI [11]. In this study, carrier signals were used in two groups. Carrier signal and reference signal are shown in Figure 2

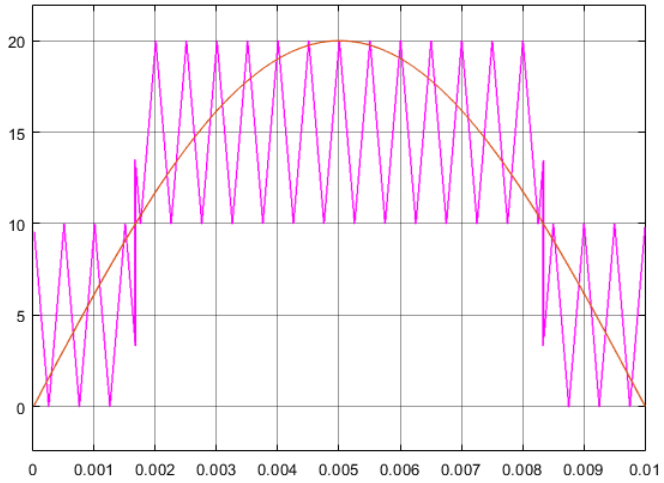

Fig. 2. Carrier signal and reference signal

Where the reference signal is larger than the carrier signal, logic-1 is formed, and where it is smaller, logic-0 is formed. The logic signals obtained as a result of the comparison of the signals in Figure 2 are shown in Figure 3.

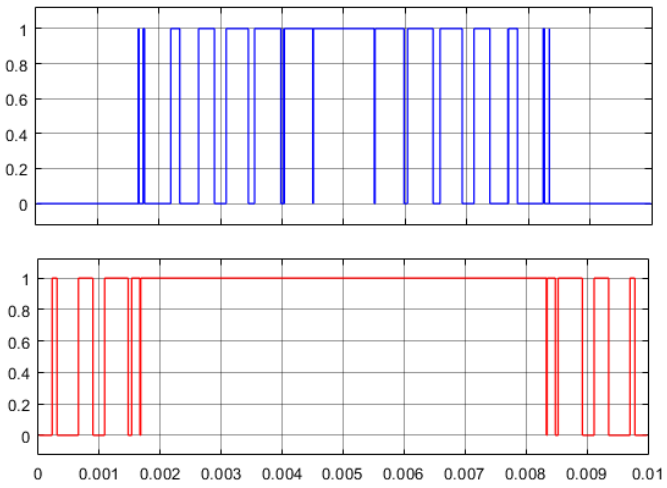

Fig. 3. SPWM signals

As shown in Figure 3, for 5-level inverter, 2 fundamental signals are generated and routed to different switches for positive and negative loop.

XSG blocks are used in the MATLAB/Simulink environment, the inverter algorithm required to generate the signals. If no equivalent block is found, C-based MATLAB code is written using the MCode block or HDL code is written using the Black Box block. Therefore, since there is no equivalent block in this study, the necessary signal is generated using the MCode block. Figure 4 shows the control algorithm created with XSG block sets.

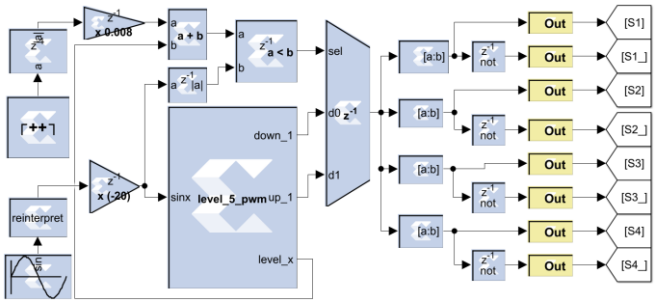

Fig. 4. XSG blocks used to create HDL code

HDL codes are created with the blocks shown in Figure 4 and loaded onto the FPGA development board via VIVADO.

The output voltage in the NPC-MLI circuit is applied to a 100Ω load. In Figure 5, the voltage measured at the load is shown with filter and without filter. The fundamental component and THD values of the output current are shown in Figure 6 and Figure 7 using a 20mH filter.

IV. IV. RESULTS

A simulation study of 5-level single-phase NPC-MLI topology was carried out using the power circuit with the blocks in the MATLAB/Simulink environment and the signal circuit with the XSG block sets. The parameters used for the simulation study of the NPC-MLI topology are given in Table 2.

Table 2. Simulation specification

Parameter	Value
DC Input Voltages	800V
Output Voltage Frequency	50Hz
Switching Frequency	20kHz
Load	100Ω
Filter	20mH

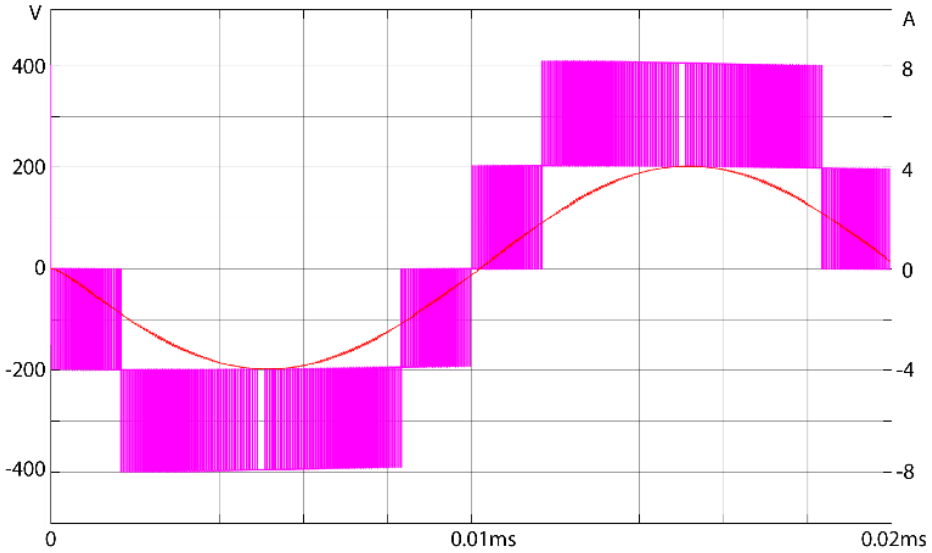

Fig. 5. Output voltage and current

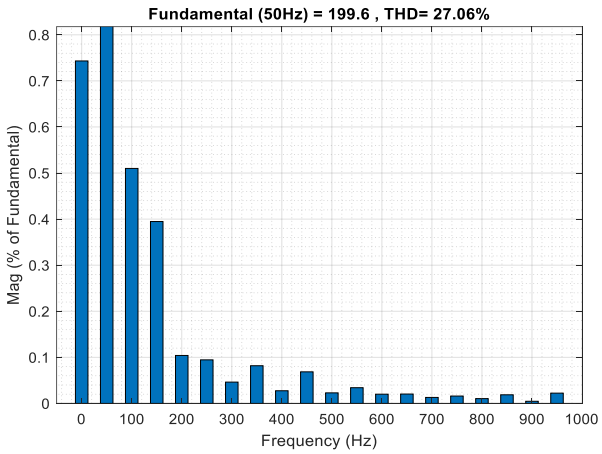

Fig. 6. FFT and THD analysis for R load with filter

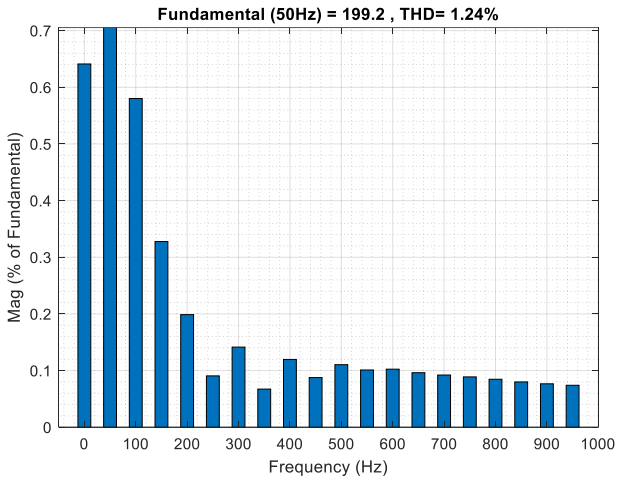

Fig 7. FFT and THD analysis for R load without filter

Figure 8 shows two main signals obtained from MATLAB/Simulink for driving switching components in NPC-MLI topology. The other two are phase shifts of the main signals.

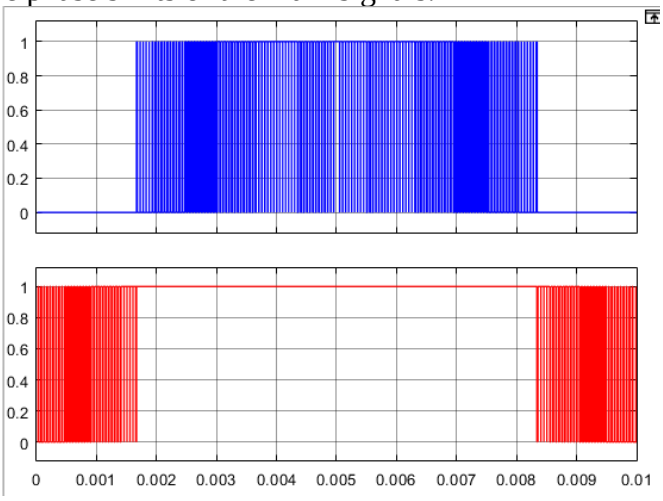

Fig. 8. Gate signals in MATLAB/Simulink

In Figure 9, the gate signals obtained from the FPGA board are shown.

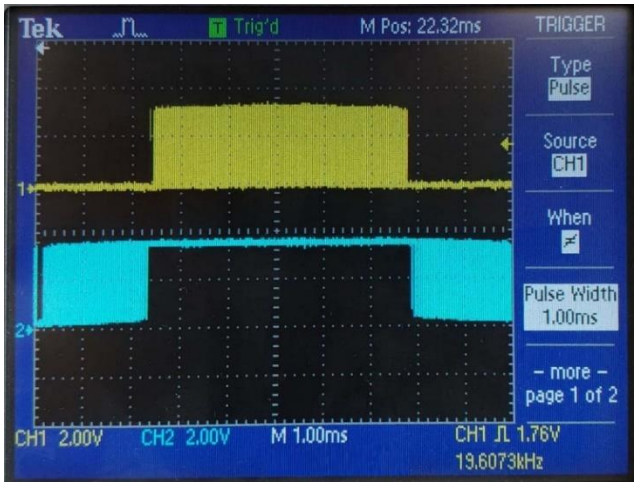

Fig. 9. Gate signals on the oscilloscope

The signals obtained in Figure 9 confirm the signals in Figure 8. The voltage of the FPGA output signals is 3.3V. Therefore, a high-side, low-side driver must be used to amplify signals to 15V. The output of the driver can be applied to the switches.

V. CONCLUSION

In this study, a fast signal generation using SPWM technique for 5-level single-phase NPC-MLI using FPGA is demonstrated. The fast and parallel operation of the FPGA provides a suitable platform for generating fast switching signals required for complex switching schemes of multilevel inverters. The production of HDL code with MATLAB/Simulink, which even qualified engineers have difficulty, is shown. Analyzes and simulations made in MATLAB/Simulink environment show that SPWM technique can be used successfully on NPC-MLI inverter and we can obtain the desired level of harmonic distortion on the output voltage. The signals transmitted to the switching elements in the topology are verified with the oscilloscope. The THD of the output current has been reduced from 27% without filter to 1.24% with a 20mH inductor.

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