

## Analysis on the capacitance characteristics of an Au/WO<sub>x</sub>/nSi junction

Murat GÜLNAHAR\*<sup>1</sup>

<sup>1</sup>Department of Electrics/Vocational School, Erzincan Binali Yıldırım University, Turkey

\*mgulnahaer@erzincan.edu.tr Email of the corresponding author

**Abstract** – In this work, an Au/WO<sub>x</sub>/n-Si metal-semiconductor device (MIS) have been realized by the fabrication using the thermal evaporation deposition procedure of WO<sub>x</sub> thin films on n-cSi. To analyze the electronic structure properties of Au/WO<sub>x</sub>/n-Si has been used the C-V and G-V measurement techniques at room temperature and for the frequencies which are 250 kHz, 500 kHz, 750 kHz and 1 MHz. The capacitance peaks viewed dependent to the applied frequency of Au/WO<sub>x</sub>/n-Si sample have been attributed to the bulk trapped charges and the interface states. In addition, it was seen that the capacitance curve of the depletion region under the illumination are the lower capacitance peak than the other capacitance curve which is non-illuminated. In result, it was noted that the illumination is effective on the capacitance curves and their peaks.

**Keywords** – Tmos, Capacitance-Voltage Characteristics, Schottky Diodes, Conductance, Interface Charges

### I. INTRODUCTION

The Molybdenum Oxide (MoO<sub>x</sub>), Vanadium Oxide (V<sub>2</sub>O<sub>x</sub>), and Tungsten Oxide (WO<sub>x</sub>) are Transitional Metal Oxide (TMO) and so far, they have been the subject of intense research interests among the photovoltaic community [1,2]. TMOs has had a big attention due to extraordinary electrical and optical properties which are structural, such as high transparency in the large work function, visible light range, and the presence of electronic states [3]. Moreover, these structures have been the acting as a hole-selective layer in organic and inorganic electronic/optoelectronic devices [15]. Due to their larger work function (> 5.5 eV) and wider band gap (> 3 eV), they have been a charge transport layer for holes in c-Si heterojunction (SHJ) solar cell designs [4]. Besides, the wide band gap of TMOs has allowed to enhanced optical transmittance which decreases the intrinsic optical absorption of the spectrum. As a result, these materials can move as a window layer in tandem with the transparent conducting oxides in SHJ solar designs [4,5].

Among TMOs materials, although MoO<sub>x</sub> has been widely studied in the literature [4,6], WO<sub>x</sub> based PV devices have been the lower prevalence of [7]. Due to a corresponding decrease in the oxidation state that simultaneously decreased the transparency and work function of the material, the conductivity of WO<sub>x</sub> increase [6]. Thus, WO<sub>x</sub> films as hole-selective contacts have been a candidate for PV applications.

To the best of our knowledge, the capacitance properties related to WO<sub>x</sub> material has been rarely reported in the literature [7]. In this study, the voltage-dependent capacitance and conductance characteristics of MIS capacitors based on Au/WO<sub>x</sub>/n-Si are investigated at room temperature with a frequency range of 250 kHz to 1 MHz. From the frequency-dependent capacitance-voltage (C-V) curves, the separate peak behaviors in depletion and inversion regimes for Au/WO<sub>x</sub>/n-Si capacitor were determined. The loss ( $L = G/\omega$ ) curves for depletion region of the studied capacitor sample were characterized. In addition, the illuminated and non-illuminated C-V curves of Au/WO<sub>x</sub>/n-Si device are analyzed. Therefore, in this work, it is realized in-

depth analysis of the capacitance properties for Au/WO<sub>x</sub>/n-Si capacitor.

## II. MATERIALS AND METHOD

The fabrication operation of WO<sub>x</sub> based Au/WO<sub>x</sub>/n-Si junction were performed by thermal evaporation on 1-3 Ω.cm n-type (100) Fz c-Si wafers. In addition, WO<sub>x</sub> thin films deposited by vacuum sublimation in this work have 99.99% WO<sub>x</sub> powder purity. RCA1 and RCA2 procedures were applied for the cleaning of the wafers. After completing the rear side HF treatment process for our sample, full-area golden (Au) and full-area aluminum (Al) operations were realized by thermally evaporation technique on n-Si substrate, respectively, with the thickness of ~ 250 nm. The thermal evaporation system was vacuumed to ~ 2x10<sup>-6</sup> Torr in whole our deposition procedures. To complete the MIS devices, Au Schott contacts were made by the deposition on WO<sub>x</sub> through a shadow mask having circular openings with a diameter of 0,5 mm. Room temperature C-V measurements were collected by an automated measurement system using an Impedance Analyzer.

## III. RESULT AND DISCUSSION

The schematic configuration of Au/WO<sub>x</sub>/n-Si device is presented in Fig. 1. Here,  $C_i$  is the insulator layer capacitance,  $C_d$  is the capacitance of the semiconductor depletion layer,  $C_{it}$  and  $R_{it}$  are respectively the capacitance and resistance of the interface trap levels,  $C_b$  and  $R_b$  are the capacitance and resistance of the n-type Si semiconductor, respectively, and  $R_c$  is the rear (ohmic) layer resistance.

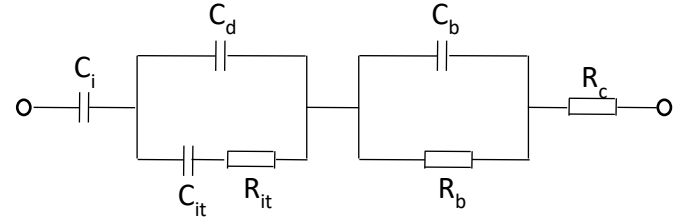
The capacitance of the insulator layer  $C_i$  can be determined by using of the expression given by:

$$C_i = \frac{\epsilon_i \epsilon_0 A}{d_i} \quad (1)$$

where  $\epsilon_i$  is the dielectric constant of the insulator layer,  $\epsilon_0$  is the dielectric constant of vacuum, A is the area of the MIS capacitor, and  $d_i$  is the thickness of the insulator layer. In this case, the measured capacitance may be affected due to the capacitance of the WO<sub>x</sub> and this capacitance can be obtained by:

$$C_{WO_x} = \frac{\epsilon_{WO_x} \epsilon_0 A}{d_{WO_x}} \quad (2)$$

where  $\epsilon_{WO_x}$  is WO<sub>x</sub> the dielectric constant of WO<sub>x</sub> layer,  $d_{WO_x}$  is the thickness of the WO<sub>x</sub>, and  $C_{WO_x}$

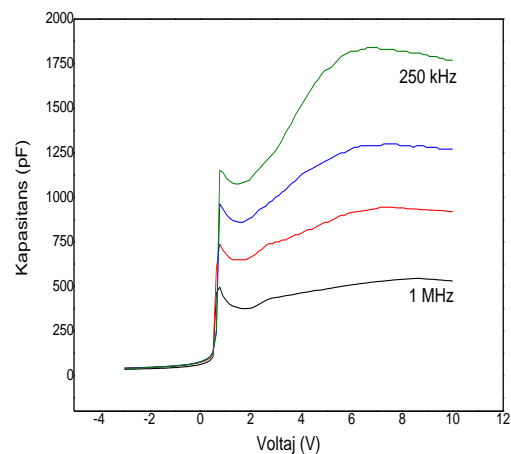


Şekil 1. The equivalent circuit structure of Au/WO<sub>x</sub>/nSi device.

is the geometric capacitance of the WO<sub>x</sub>.  $C_{WO_x}$  in this work is calculated to be  $8.15 \times 10^{-9}$  F from Eq. (2). Moreover, the capacitance for WO<sub>x</sub> being operated in the full depletion regime is the equal to:

$$\frac{1}{C} = \frac{1}{C_i} + \frac{1}{C_{WO_x}} \quad (3)$$

In addition, the capacitance of depleted layer  $C_d$  can be obtained from the equation which is  $C_d = \epsilon_s \epsilon_0 A / w_s$  where  $w_s$  is the width of depletion layer can be determined from that can be obtained from  $w_s = \sqrt{2 \epsilon_s \epsilon_0 V_0 / qN}$ , where  $\epsilon_s$  is the dielectric constant of the semiconductor,  $N$  is net ionized state density which is the  $N_d - N_a$  for n-Si and  $V_0$  is the diffusion potential.



Şekil 2. The capacitance-voltage characteristics measured at 250 kHz, 500 kHz, 750 kHz and 1 MHz frequencies of Au/WO<sub>x</sub>/nSi device.

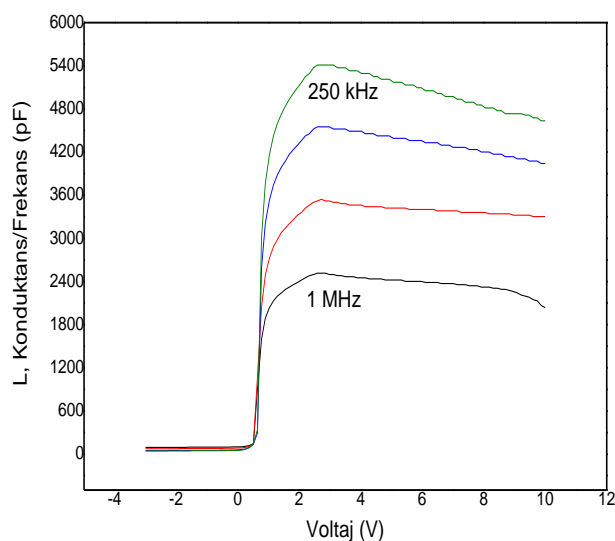
The C-V characteristics of MIS capacitor based on an Au/WO<sub>x</sub>/n-Si heterojunction structure have been measured at various frequencies. Fig.2 shows the C-V curves for the C-V analysis at various AC frequencies as 1 MHz, 750 kHz, 500 kHz and 250 kHz of Au/WO<sub>x</sub>/n-Si device, at room temperature, in the applied voltage between from -3 to 10 V.

The shapes of the C-V profiles measured at all frequencies of n-Si based on device are different and n-Si based device exhibit peaks at positive voltages in Fig. 2. The capacitance values were appeared to be constant at ~ 0 V value and at negative biases for Au/WO<sub>x</sub>/n-Si junction. In addition, the capacitance values of Au/WO<sub>x</sub>/n-Si have started to decline rapidly with an increasing frequency after the maximum peak positions at low frequencies. In Fig. 2, C-V curves of Au/WO<sub>x</sub>/n-Si sample have demonstrated the accumulation, depletion, and inversion regions for each frequency step. The capacitance values have increased with decreasing frequency in the forward voltage region and in result, they have transformed to the peaks like to the shoulder with decreasing frequency, at its inversion region.

The general peak behaviors in C-V curves of Ag/WO<sub>x</sub>/n-Si and Ag/WO<sub>x</sub>/p-Si heterojunctions in Figs. 2 and 3 demonstrate the similarity to the capacitance peaks of MoO<sub>3</sub>/n-Si and MoO<sub>3</sub>/p-Si devices characterized for low frequencies in [6].

The loss equation expressed as  $L = G/\omega$  yields the normalized conductance values determined from where  $G$  is the conductance and  $\omega$  is the frequency. Fig. 3 presents the L-V curves for Au/WO<sub>x</sub>/n-Si sample. From Fig. 3, it is seen that the L-V characteristics of the Au/WO<sub>x</sub>/n-Si sample have exhibited gradual shift in the peak profile within its forward bias regime in the frequencies below 1 MHz. In the frequencies lower than 1 MHz,  $L$  curves increase in the depletion region of the device.

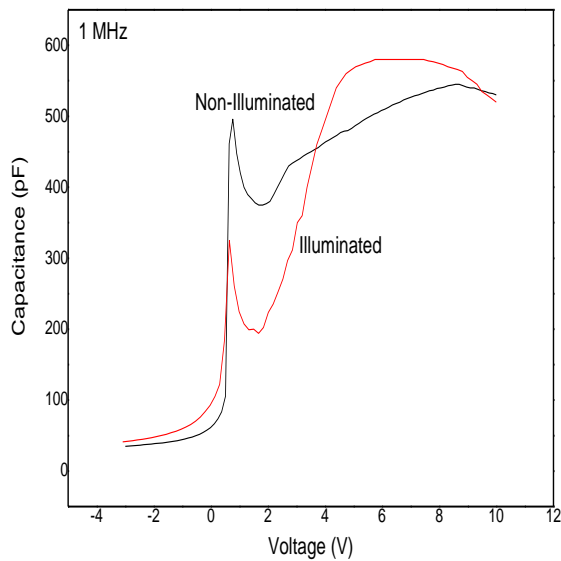
From Figs. 2 and 3, it can be explained that the curves of C-V and L-V for Au/WO<sub>x</sub>/n-Si sample were affected from the applied frequency and bias. The many parameters such as series resistance, surface polarization, the density distribution of the interface states, deep traps within the depletion region, minority carriers concentration, and the contribution of interface traps [6], both C capacitance and L loss values induce as the



Şekil 3. The loss (conductance/frequency) characteristics measured at 250 kHz, 500 kHz, 750 kHz and 1 MHz frequencies of Au/WO<sub>x</sub>/nSi device.

different peaks. There is an oxide layer formed between c-Si and WO<sub>x</sub> in our junction and it is occupied by the interface traps [7]. Schottky junctions affect from the interface layer in which the interface states give rise to the formation of the vacancies, acceptor or donor traps, and generation-recombination centers. Furthermore, the interface states have one or more energy levels deposited within the band gap of c-Si. The Shockley-Read-Hall center that exists at the interface and the bulk, determine the interface trap level density [3]. Due to an enhanced movement of charge carriers, more defects states may be formed that reduce the mobility and the charge carrier concentration.

The whole device featuring Au/WO<sub>x</sub>/n-Si sample can be considered as a combination of two separate capacitors comprising the depletion layer and the bulk c-Si semiconductor. The electrons and holes are the mobile charge carriers in the semiconductors. In case of the n-type semiconductor, the majority carrier concentration is larger than the hole concentration. C-V data may be influenced the mobility of majority charge carriers due to the frequency of the applied external signal the frequency of the applied external signal. When the bulk trap charge density being larger than that of the interface charge density, some peak appearances have been noted to appear such as the



Şekil 4. The illuminated and non- illuminated capacitance-voltage curves at 1 MHz frequency of Au/WO<sub>x</sub>/nSi capacitor.

weak inversion regime [4]. Consequently, the peak formation in the weak inversion regime may be due to the bulk trapped charges rather than the interface states. In our case, the peaks depicted in the inversion regime of C-V data in Fig. 2 and L-V data in Fig. 3 for Au/WO<sub>x</sub>/n-Si junction may be related to the c-Si bulk, mobile charge carriers and bulk trapped charges. This result approves the experimental results in [2] in which the peaks maximums appear while interface charge density is lower than that of bulk trap charge. The peak maxima in the depletion region of Au/WO<sub>x</sub>/n-Si belong to the presence of the interface trapped charges in addition to the depletion capacitance. This difference can be attributed to the contribution of the interface trapped charges in the capacitance of the device, as explained for the experimental observations in [5].

In addition, to represent the effect of the illumination on C-V measurements were made the capacitance measurements under the illumination. Fig. 4 presents both of the C-V data which is the illuminated and non-illuminated to compare at 1 MHz. Compared to that of both of them in Fig.4, it is seen that the depletion capacitance regime of the C-V curves under the illumination according to the depletion capacitance regime of the non-illumination C-V curves have the C-V peak formation which is the lower. However, the

accumulation capacitance regime due to the bulk capacitance effect for every two situation is the opposite of this condition. The bulk semiconductor peak under the illumination is the larger and bigger than the other peak formation. This result clearly express that the contribution of the interface trapped charges in the capacitance of the device decrease due to the illumination effect. However, the effect of the bulk charges increase by the illumination effect and it concludes with the increasing of the bulk capacitance in the accumulation regime.

#### IV. CONCLUSION

The electronic structure of a MIS capacitor based on Au/WO<sub>x</sub>/n-Si has been investigated by C-V and G-V measurements at room temperature and for the frequencies which are 250 kHz, 500 kHz, 750 kHz and 1 MHz. The capacitance peaks viewed at lower frequencies in the weak inversion region of Au/WO<sub>x</sub>/n-Si capacitor have been related to the bulk trapped charges and the interface states. From the illuminated and non-illuminated C-V characteristics, the capacitance curve of the depletion region under the illumination has the lower capacitance peak than the other capacitance curve, on the contrary for the inversion layer, compared to that of both capacitance curves.

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