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Research Article

Design of an integrated SEPIC and Buck Converter for High Step-down Applications

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Abstract – To overcome the issues related to special power supply called voltage regulator module (VRM) used for microprocessors, a special DC-DC converter will be designed in this work in which single-ended primary inductor (SEPIC) converter and the inverted form of buck converter are combine. As per available literature the problems associated with conventional VRM's are slow transient response and narrow duty cycle. Other issue related to the voltage regulator module is the high voltage stress that occurs on switches of VRM. The solution to these problems is presented in the form of a new proposed dc-dc converter topology in which the single ended primary inductor is combined with the inverted form of buck converter. The proposed topology has the advantages of reducing the transient time at moderate duty cycle because of the parallel combination of the inductor. Similarly, the parallel combination of capacitor will step down the voltage from 12v to the appropriate voltage level required for the microprocessor. The steady state operation and transient state operation of the proposed VRM is discussed in this thesis. Various operating states of proposed converter are discussed and related equations for voltage gain, voltage stress and transient response have been derived. Output waveforms are plotted, and mathematical modeling is carried out. Simulation results for proposed and conventional VRM are obtained and from comparison of results, it is clear that proposed VRM is good in performances compared to conventional VRM's.

Keywords - Buck Converter, Interleaved Buck Converter, Step-Down Voltage Conversion Ratio.

I. INTRODUCTION

The Voltage regulator module (VRM) also sometimes referred to as the processor power module or the PPM falls under the category of electronic circuit. Its principal functionality is to supply adequate voltage to the microprocessor. For the purpose of achieving this goal, the VRM manipulates its input voltage by regulating and stepping it down to the integrated circuit which is the output. The imperative functionality of the

regulator module is to determine the voltage requirement of the microprocessor through sensors and make sure that the accurate voltage is maintained. More often, the voltage regulators modules are used in application of switching regulator (also known as the buck converter) because of their efficiency.

To fulfil the requirement of the modern microprocessor, VRM based buck, synchronous buck and related topologies are utilized. Typically, buck converters are capitalized in designing of VRM but this is not the only approach for it. Figure (1.1) illustrates the VRM circuits' basic schematics. On the left side, is the PSU or the Power supply unit supplying voltage of 12 volt The circuit involves two MOSFETS switches; low side and high side. Two points in the figure are mentioned as A and B. On the left side of the point B; is the filtering inductor.

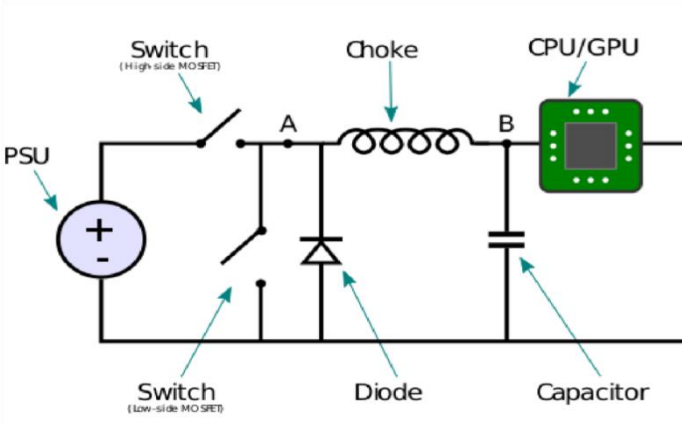


Figure 1 Basic Buck Converter

The purpose of this circuit is to lower the input voltage which is 12V enough for operating voltage of the CPU/GPU .The terminal goal of the circuit is to provide perpetual voltage of desired magnitude. Today's microprocessor requires low voltage; approximately 1.2V. For this purpose, cutting off the inductor charging is required by the circuit when the voltage hits 1.2V mark at point B. Upon happening so, the voltage will drop. At this stage, the inductor charging will start again as per circuit design [1]. This cycle will be repeated indefinitely because of a technique known as Pulse Width Modulation (PWM). At approximately 50% duty cycle mark, the output voltage at point referred in the circuit as point B will be approximately half (6V) of the input voltage (12V). In order to achieve the desired voltage which is 1.2V, we need to set the duty cycle to10%. In real-world circuits, PWM controllers are used with a driver for the opening and shutting of the low-side and high-side switches (MOSFETs).

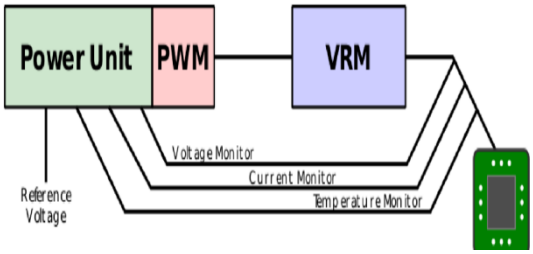


Figure 2 Feedback and regulation of VRM

The figure 1.2 above shows that the VRM comprises of some basic components namely MOSFETs, Capacitors and Chokes etc. The power unit falls under PWM controller as its part. However, the mechanics of both is almost same. The power supply provides a reference voltage which is then connected to the unit and after that, the unit is compared with monitored voltage. The PWM signal is modified through the difference between the reference voltage, the desired voltage and the real voltage which is fed to the CPU. This ensures that the real signal is fed to the CPU. Consistent sampling is carried out after intervals for a given period of time. The goal is to deliver voltage to the load that is as near as possible to the reference voltage [2].

At the point when Intel proposed the Pentium 2 chip the silver box, which was the first control supply structure could never again fulfil the new processor's requirement of modest effectiveness with high current and quick transient reaction with tight resistance [7]. An exceptional dc– dc converter, the voltage controller module (VRM), which can be put in favour of the processor, was created as a power supply changing over 5 V to about 2.8 V [8]. In view of its basic structure, the

buck converter with a synchronous rectifier is utilized for the VRM plan.

When the switching circuit is ON, the power supply voltage is supplied to the coil, and when it is OFF, the switching circuit is grounded to emit the energy accumulated in the coil. The synchronous rectifier circuit controls ON / OFF timing by using MOSFET. When the switches are turned on at the meantime, they are shorted, so they must be synchronized and turned on / off without fail. In the multiphase synchronous rectifier circuit, a plurality of switching circuits is prepared and the switches are sequentially turned on / off. Power consumption differs greatly between the CPU and other devices. For this reason, various measures have been taken for the power supply circuit used for the VRM, which are greatly related to the grade of the motherboard product. Costly motherboards use circuits costly to VRM. Let's focus on the VRM for CPU, first explain the circuit configuration of VRM and main components [9]. If we join 2 buck converters, the circuit becomes a Quadratic buck converter. In this circuit, although the voltage levels are high, but the transient response is fast, although in 2 separate Buck converters, the voltage stress is reduced [10]. A common diode connects the secondary and primary winding in a tapped inductor buck converter. To manage switching and conduction losses, the duty cycle must be controlled. However, the disadvantage of this circuit is that, it gives rise to very high voltage. Similarly, in a coupled inductor buck converter, the current ripples are decreased, which is one of its major advantages. The switching and conduction losses are reduced, and efficiency is quite enhanced at the same time with the utilization of 4 Interleaved and coupled inductors [11]. The venturing inductance technique is actualized by replacing the ordinary inductor in a buck converter by two inductors interfacing in arrangement. One has extensive inductance and alternate has little inductance. The inductor with little inductance will assume control over the yield inductor amid transient load switch and accelerate dynamic reaction. In consistent express the extensive inductance assumes control and keeps a generously little swell current and limits root mean square misfortune. It is an ease technique relevant to converters with a yield inductor [12, 13]. The voltage controller module in this classification utilizes multiphase synchronous Buck converter for providing extensive load flows. The information and yield voltages in the VRM reproduction are individually 8.5 V and 1V separately. The reproduction circuit utilizes a solitary stage comparable circuit for re-enactment with twofold capacitors in the information and yield circuits to represent real qualities utilized per stage [14]. The low voltage and higher current requests of the future chip could severely affect the nature of intensity conveyed to the CPU. Because of the unusual voltage drop caused by an expansive current at this point in the link, an exact voltage control and a great transient reaction are extremely troublesome accomplished. The way to deal with defeat this issue is to turn to the point-or-Load direction strategy, famously known as the voltage controller module (VRM) [15].

PROPOSED MODEL

To introduce a new topology of a DC-DC Interleaved buck converter which is more suitable, efficient, and lower in cost as compared to other traditional buck converters available in the present market which have more power losses, are less efficient, high in price, and component maintenance is difficult due to the old-school components used in conventional converters, which result in high power losses. The design of a new converter contains a proper procedure to convert the idea of a new converter into a physical shape and use it for suitable devices. The first step for the new topology is to collect the related data about the voltage regulators and analyze the conventional converters' duty cycles, voltage ripples, current ripples, efficiency, etc. The proposed converter is introduced. The aim of this new topology is that the world is going to moveto a new technology invented day-by-day which is more suitable and efficient in today’shours. Therefore, we introduce a new topology which is more efficient. Similarly, find out the switching states and do the mathematical calculations for a proposed converter to achieve the proposed circuit characteristics and formula through which all the calculations for a new converter are to be done. The formula for a new converter is obtained, and through this, all the requirements of a project can be solved. In the next step, a simulation of a proposed converter takes place in MATLAB Simulink to achieve results, i.e.,

component values (capacitor & inductor), voltage & current ripples, and the comparative analysis to achieve circuit goals. The finalized all the values of the capacitors & inductors used in the proposed converter and moved to a stage implementation. The circuit is implemented practically, and the experimental results are obtained.

A. Proposed Converter

To step down the output voltage and match the project criteria, we presented a new topology of a DC-DC converter based on the briefly described information. A high inputvoltage is converted to a low output voltage in the proposed converter, which is also an interleaved DC-DC buck converter. The suggested converter has two phases, the first of which employs a conventional SEPIC converter and the second of which uses an inverted buck converter. Compared to the conventional interleaved converters, this method allows for a high step-down voltage conversion. A similar interleaved buck converter, Figure 2.8, has the drawback of having the output polarity inverted, as opposed to the proposed converter's input polarity. Due to its extremely low voltage andcurrent ripple and high conversion ratio at the same duty cycle as the other converter used to step down the voltage, it is also more efficient.

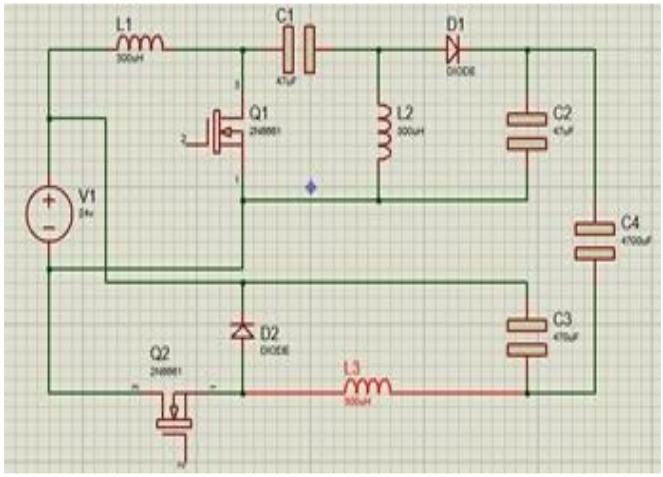
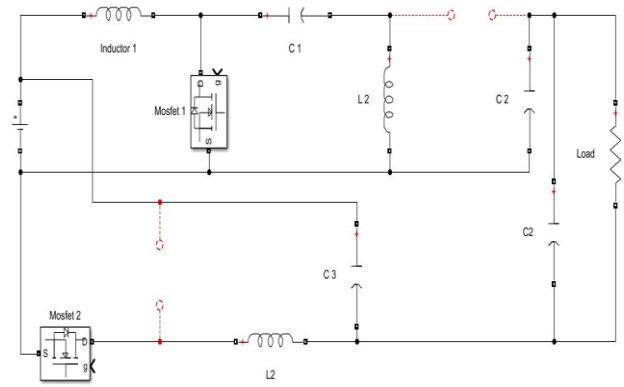
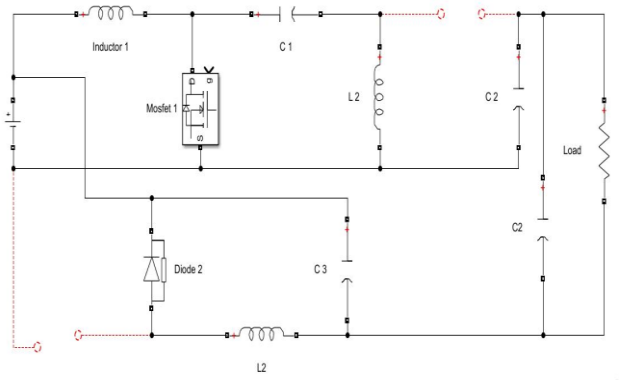


Figure 3 Proposed Converters

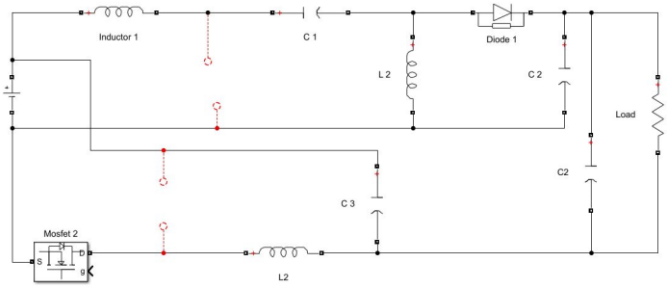
Operating Principal of Proposed System



(a)



(b)



(c)

Figure 3.1 Operating switching States, (a) State I and State III, (b) State II, (c) State IV

Switching Operation State-I

State-I starts at initiative time of t = t0. During operation of State-I Switch 1 and switch 2 are at ON. Switching used are actually MOSFET. Rather than that diode 1 and diode 2 are at OFF state. The circuit diagram for State-I operation is shown in figure 3.1(a).

Switching Operation State-II

This operation state began with switch 1 at ON state and switch 2 at OFF state. Whereas diode-1 is at OFF state and diode-2 is at ON state. the circuit diagram of operating switching State-II is given in figure 3.1(b).

Switching Operation State-III

Switching operation of State-III is same as switch operation of State-I, which is having MOSFET-1 and MOSFET-2 at ON state and diode-1 and diode-2 at OFF state. The switching operation of State-III is given in figure 3.1(a).

Switching Operation State-IV

At switching operation of State-IV the MOSFET-1 or switch-1 is at OFF state and Switch-2 is at ON state. While as diode-1 at this state is at ON state and diode-2 is at OFF state. The switching of this state i-e State-IV is given in Figure 3.1(c).

Proposed System Steady state analysis

State-I from Figure-3.1(a) is having the following mathematical form:

VL1 = VS

VL2 = -VC1

VL3 = V3 - VC3

State-II from Figure-3.1(b) is having mathematical form as below:

VL1 = V3

VL2 = -VC1

VL3 = -VC3

State-III from Figure 3.1(a) is having same mathematical formulations as State operation of State-I which is given as below:

VL1 = VS

VL2 = -VC1

VL3 = V3 - VC3

State-IV from Figure 3.1(c) is having mathematical formulations as below:

VL1 = VS - VC1 - VC2

VL2 = -VC3

VL3 = VS - VC3

a) Mathematical Equation:

The mathematical formula derived from the steady state analysis for the proposed converter is given below:

Vout = VO = VC2 + VC3 – VS

By voltage calculations of VL1, VL2 and VL3 we get:

$$Vo = \frac{(3D-D^2-1)}{(1-D)} * Vs \quad \ldots\ldots\ldots\ldots (1)$$

b) Mathematical Calculation:

Equation (1) is used for calculating the output voltage *Vo* of a proposed converter byputting the value of a duty ratio and input supply voltage:

Duty ratio, D = 45 % = 0.45 & Input voltage,

Vs = 24 volts put in Eq. 1, we get;

$$Vo = \frac{[3(0.45) - (0.45)^2 - 1]}{(1 - 0.45)} * 24V$$

$$Vo = \frac{1.35 - 0.2025 - 1]}{0.55} * 24V$$

$$Vo = 6.1\ volts \ldots\ldots\ldots (2)$$

Eq. 2 shows the theoretical output voltage of a proposed converter.

Parameters used for Simulation

Table .1: Parameters of SEPIC Converter

Names of Parameters	Symbol	Quantity	Value
Input Voltage	V_s	-	24 V
Duty Ratio	D	-	0.45
Switching Frequency	F_s	-	35 KHz
Inductor	L	2	300 µH
Capacitor	C	2	47 µF

Table 2: Parameters of Inverted Buck Converter

Names of Parameters	Symbol	Quantity	Value
Input Voltage	V_s	-	24 V
Duty Ratio	D	-	0.45
Switching Frequency	F_s	-	35 KHz
Inductor	L	1	300 µH
Capacitor	C	1	47 µF

Table 3: Parameters of Proposed Converter

Names of Parameters	Symbol	Quantity	Value
Input Voltage	V_s	-	24 V
Duty Ratio	D	-	0.45
Switching Frequency	F_s	-	35 KHz
Inductor	L	3	300 µH
Capacitor	C	3	$C_{1,2}$ = 47 µF, C_3 = 470 µF
Output Filtering Capacitor	C_o	1	4700 µF

II. SIMULATION RESULTS

The findings of our project's implementation are as follows: the SEPIC converter's output voltage is 18.86 volts, its voltage ripples are 0.08, and its current ripples are 0.004. The inverted buck converter's output voltage is 10.33 volts, and its waves in voltage and current ripples are 0.07 and 0.0063, respectively. The output voltage of a proposed converter is 5 volts, where the input supply voltage is 24 volts. The proposedconverter has relatively low voltage ripples 0.006 and current ripples 0.0011 when compared to the two individual converters. The simulation results, including the voltage and current graphs and a comparison of all three converters, which are given below, along with a description of the converter's hardware implementation

1) Results

To analyze the outcomes of simulation, the simulation results for all three converter SEPIC converter, inverted buck converter, and proposed converter are provided in graphical and tabular formats.

V. Graphs of SEPIC Converter

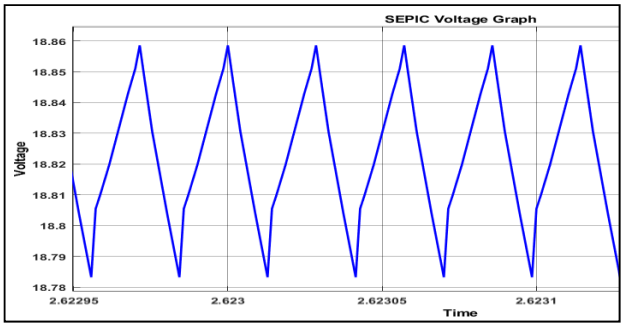


Figure 4 Voltage Graph of SEPIC Converter

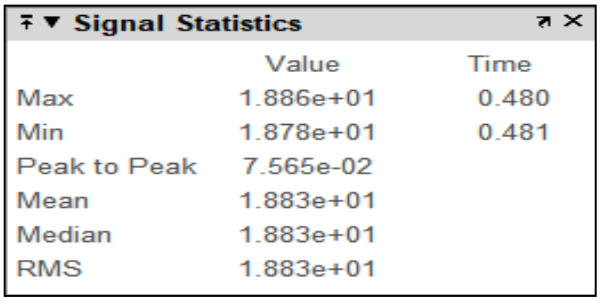


Figure 5 Voltage Signal Statistics of SEPIC Converter

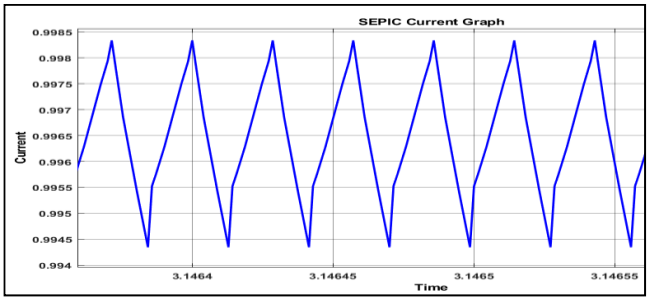


Figure 6 Current Graph of SEPIC Converter

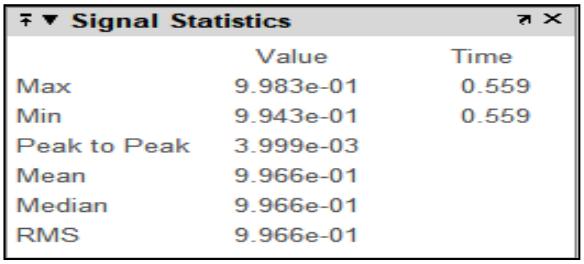


Figure 7 Current Graph of SEPIC Converter

All the above figures are i-e Figures 4, 5, 6, & 7 shows the simulation results of the conventional SEPIC converter. Figure 4 indicates the output voltage waveform of a SEPIC converter, and Figure 5 shows the signal statistics of the output voltage waveform from where the voltage ripples are calculated. Similarly, Figure 6 shows the output current waveform of a SEPIC converter, and Figure 7 shows the signal statistics of the output current waveform from where the current ripples of the SEPIC converter are calculated. The below Table 4 shows the simulated output voltage and current values along with the calculated voltage and current ripple values of a SEPIC converter.

Table 4: Simulation Results of SEPIC Converter

SEPIC Converter			
Output Voltage V_o	Voltage Ripples □V	Output Current I_o	Current Ripples □I
18.86 V	0.08	0.9986 A	0.004

VI Graphs of Inverted Buck

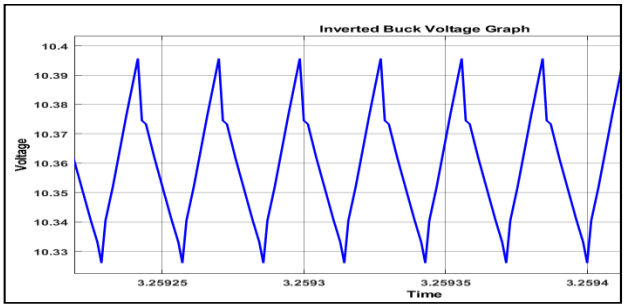


Figure 8 Voltage Graph of Inverted Buck Converter

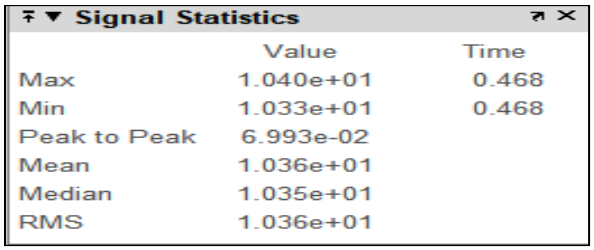


Figure 9: Voltage Signal Statistics of Inverted Buck Converter

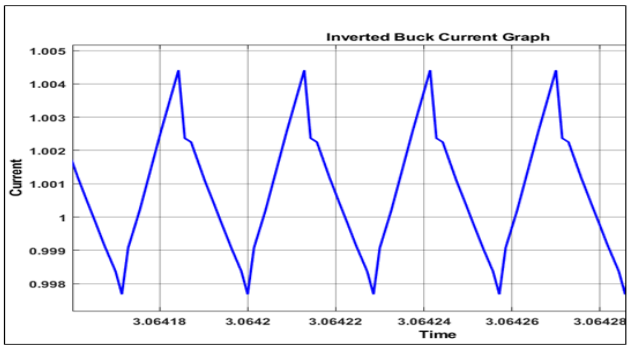


Figure 10: Current Graph of Inverted Buck converter.

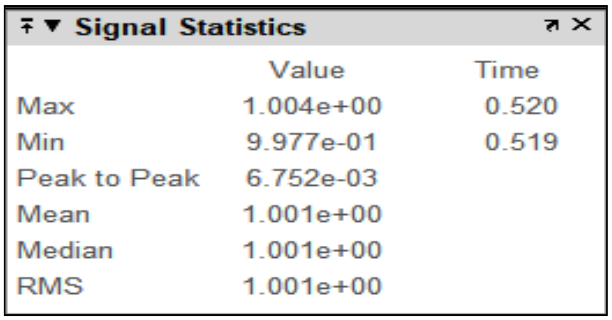


Figure 11: Current Signal Statistics of Inverted Buck Converter

All the above figures are i-e Figure 8, 9, 10, & 11 show the simulation results of an inverted buck converter Figure 4.5 indicates the output voltage waveform of an inverted buck converter, and Figure 4.6 shows the signal statistics of the output voltage.

Inverted Buck Converter			
Output Voltage V_o	Voltage Ripple ΔV	Output Current I_o	Current Ripple ΔI
10.33 V	0.07	0.9977 A	0.0063

Table 5: Simulation Results of Inverted Buck Converter

a) VI Graphs of Proposed Converter:

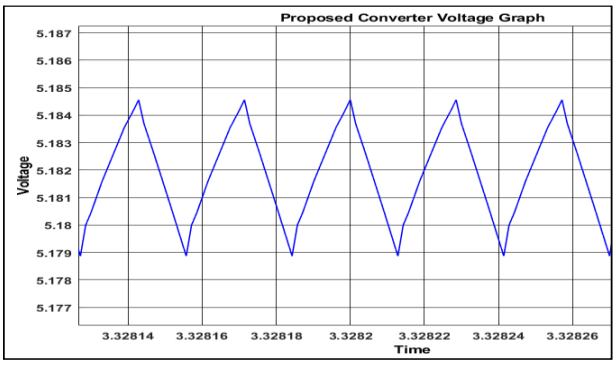


Figure 12: Voltage Graph of Proposed Converter

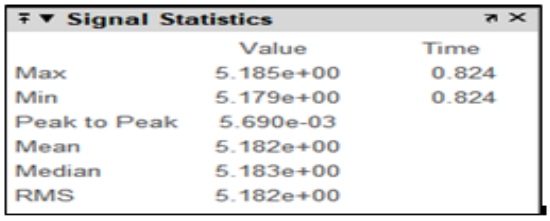


Figure 13: Voltage Signal Statistics of Proposed Converter

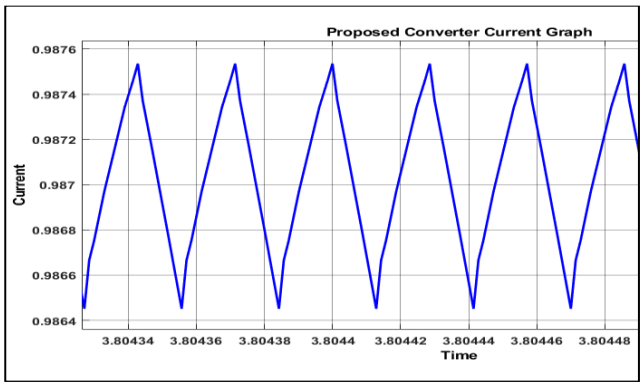


Figure 14: Current Graph of Proposed Converter

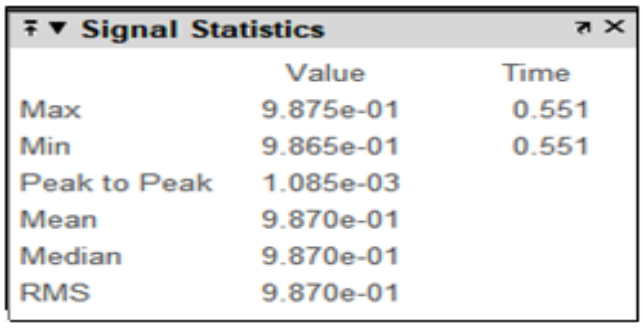


Figure 15: Current Signal Statistics of Proposed Converter

All the above figures are i-e Figures 12, 13, 14, & 15 show the simulation resultsof a proposed converter. Figure 12 indicates the output voltage waveform of a proposed converter, and Figure 13 shows the signal statistics of the output voltage waveform from where the voltage ripples are calculated. Similarly, Figure 14 shows the output current waveform, and Figure 15 shows the signal statistics of the output current waveform from where the current ripples of a proposed converter are calculated. Table 6 shows the simulated output voltage and current values along with the calculated voltage and current ripple values of a proposed converter.

Table 6: Simulation Results of Inverted Buck Converter

Proposed Converter			
Output Voltage V_o	Voltage Ripples ΔV	Output Current I_o	Current Ripples ΔI
5.185 V	0.006	0.9875 A	0.0011

COMPARISON & DİSCUSSİONS

The proposed converter is compared to conventional converters, the SEPIC, and the inverted buck converter, in Table 7. The proposed topology has a high step-down conversion ratio and low voltage and current ripples at the same duty ratio and component values that are assigned in individual simulations and then interleaved to get the proposed converter output values, as shown in the table below.

Table 7 : Comparative Analysis

Converters	Output Voltage Vo	Output Current Io	Voltage Ripples ΔV	Current Ripples ΔI
SEPIC Converter	18.86 V	0.9986 A	0.08	0.004
Buck Converter	10.33 V	0.9977 A	0.07	0.0063
Proposed Converter	5.185 V	0.9875 A	0.006	0.0011

2) Graphical Representation of Voltage Ripples:

The three converters, the SEPIC, the inverted buck, and the suggested converter, are represented graphically in Figure16. After the positive peak of the input voltage, the capacitor slowly drains through RL after charging quickly at the beginning of a cycle (when the diode is reverse-biased). The ripple voltage is the change in capacitor voltage brought on by charging and discharging. The filtering operation is better the smaller the wave because ripples are often undesired. The voltage ripples of an inverted buck converter are smaller than

those of a SEPIC converter, which has larger voltage ripples than either of the other two converters. It is evident from this that the suggested converter is superior to both existing converters in terms of suitability, efficiency, and noise level.

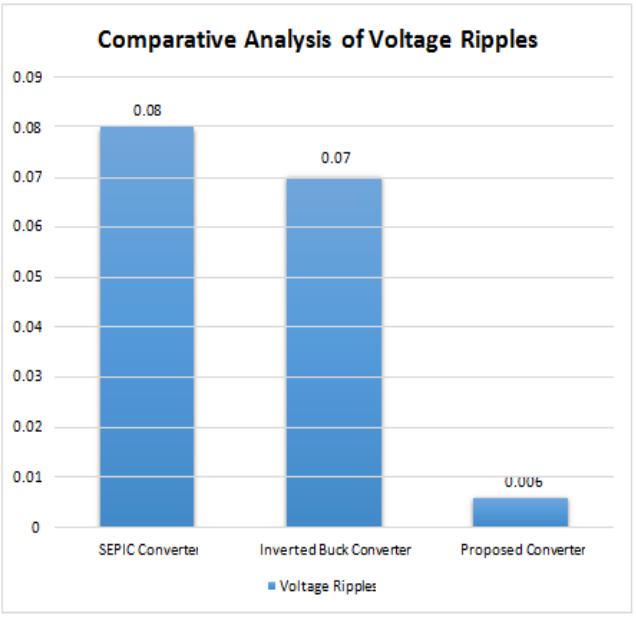


Figure 16: Voltage Ripples across the Load

Graphical Representation of Current Ripples:

The graphic representation of the current ripples produced by the three converters the SEPIC, the inverted buck, and the suggested converter can be seen in Figure 4.14. A buck converter's low-pass filter is made up of an inductor and a capacitor. In order to reduce switching ripple, the corner frequency of the LC filter is always intended to be at a low frequency. Generally, an inductor's ripple current is always planned to be closeto 30% of the average inductor current. A SEPIC converter has fewer current ripples than an inverted buck converter, while a proposed converter has significantly smaller current ripples than the other two converters combined. It is evident from this that the suggested converter is superior to both existing converters in terms of suitability, efficiency, and noise level.

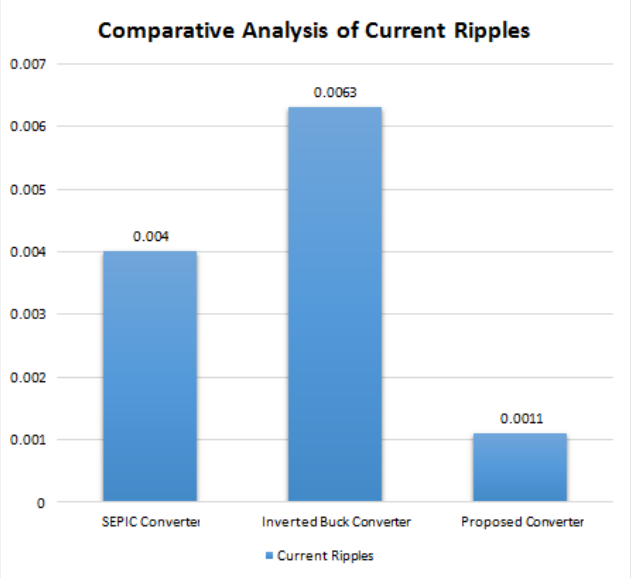


Figure 17: Current Ripples across the Load

III. CONCLUSION

This study introduced a high-step-down DC-DC converter which is the combination of a SEPIC converter and an inverted buck converter. Each converter's circuit diagram is provided, and the key ideas are covered. The reduced ripple characteristics of interleaved buck converters (IBC) have attracted a lot of interest. They do not, however, reduce the voltage conversion ratio. By using the right number of turns, tapped, and connected inductor buck converters can achieve high step-down conversion ratios, however, there is some leakage inductance that results in large voltage spikes on the switches. Without using a low-duty cycle, the switched capacitor approach can deliver a high step-down voltage. The switched capacitor converter, however, has incredibly low efficiency. High step-down voltage conversion is also achieved with switched inductor cells, however, because these cells use L-switching, the ripples are quite high. An entirely new topology of the DC-DC converter is introduced to achieve a high step-down voltage conversion. While gaining the advantages of an interleaved structure's low ripple characteristics, it can provide a better step-down conversion ratio than a conventional IBC. Interleaving helps decrease ripples in the following ways: connected inductors can minimize ripple while also extending the duty cycle; quadratic, tapped, and switched capacitors can avoid narrow duty cycles for high step-down conversion; and multilevel is helpful for lowering switch stress. The published research on non- isolated DC-DC step-down converters is thoroughly reviewed. These topologies are compared in terms of step-down conversion ratio/voltage gain, switch stresses, output current ripple, and component count. The ideal topology is chosen, and the outcomes ofthe simulation are individually provided. This project report gives students and researchers who wish to learn more about step-down DC-DC converters a clear context. The combination of a SEPIC converter with an inverted buck converter is an invention in DC-DC converters, it is concluded. It converts a 24V input to a 5V output, allowing for larger step-down voltage conversion ratios. The circuit is also more efficient and incorporates overload and short-circuit protection.

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