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Designing of Hybrid Multi-Level Inverter for Photo Voltaic Applications

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Abstract – The global surge in energy demand has highlighted the limitations of fossil fuels, both in terms of cost and availability, prompting a shift towards renewable energy sources. Developed countries are effectively managing their resources for current and future needs, while developing nations face imminent fossil fuel shortages. Renewable energy, particularly photovoltaic (PV) systems, offers a sustainable alternative due to their noiseless operation, low maintenance, and minimal environmental impact. The main challenge is the integration of renewable energy into existing AC power grids. This research focuses on incorporating PV systems to meet various power demands using a novel topology known as Multiple Levels Inverter with switch DC sources. Inverters, essential for converting DC voltage from sources like PV arrays into AC, are crucial in this process.The proposed design uses PV output as the DC input voltage, converting it into AC power via a single-phase multi-level inverter. Traditional two-level inverters suffered from issues like high total harmonic distortion (THD) and increased losses with higher levels. Multi-level inverters, however, are advantageous for high-power applications, reducing harmonic distortion and approaching a sinusoidal output waveform as levels increase. This study examines the voltage and current waveforms and evaluates total harmonic distortion in the system. Applications such as variable frequency drives (VFD), pumps, and uninterruptible power supplies (UPS) benefit from multi-level inverters. The performance of the single-phase multi-level inverter will be analyzed using MATLAB and Simulink software, providing insights into its efficacy and efficiency.

Keywords – PV,VFD,UPS,THD,AC

I. INTRODUCTION

The world is concerned about running out of energy in the future, which has sparked a lot of interest in discovering new energy-generating methods in recent years. Due to their benefits in high power, low harmonic applications, multilevel inverters have drawn large amount of attention among energy distribution and governor domain. In addition to their high power ratings, they make it possible to use renewable energy sources. A multiple-level inverter's primary job is to mix several DC voltage source. That can be generated by fuelcells, solar cells, batteries, etc.—to create the needed elevated voltage [1],[2]. Multi-level" capability refers to an inverter's ability to produce additional yield voltages level in

addition the conventional 3-level inverter. Numerous advancements in multi-level converter topologies are transpired since then [3],[4]. A multilevel converter uses a line of power semiconductor switches and several lower voltage dc sources to convert electricity into a voltage waveform that resembles a staircase. Batteries, capacitors, and renewable energy sources can all be employed to generate the various dc-voltage source. High voltage can be generating at the yield when these many direct current sources are commutated by the power switches, nevertheless, the power switches' rated voltage is entirely depending upon quality of direct current original source that are linked to [5]. Due to the large number of tiny voltages involved in switching, multilevel converters have a naturally lower rate of changes. It might therefore win out with a lower dv/dt. Multi-level inverters may provide a waveform of a stair-form voltage that is generated as the DC voltage levels rise. That might outcome in a wave that resembles a sine wave more closely. Additionally, rising amount of Dc voltage has made it easier to eliminate extra harmonic components. Removing the harmonic contents will make filtering the remaining harmonic stuff easier. Consequently, filters will be less expensive and smaller [7],[8]. Multi-level converters can use fundamental frequencies or higher-frequency flipping PWM for switching. It is important to note that efficiency increases and switching loss decreases with decreasing switching frequency. Reducing the dv/dt fluctuations will also help to lessen voltages variations per basics cycle caused by altering at the frequency of operation [9]. Many switches are needed to avoid lower voltages since multilevel inverters often use a lot of dc voltage. Switch ratings may drop as a result of shrinking switch strains. System reliability is quite good for multi-level converters. They frequently have redundancy due to switching. In other words, there can be more than one method for supplying the required voltage. A multi-level converter frequently continues to function even after a component fails, but at a lower power level [10], [11]. Multilevel inverters do indeed had enough disadvantages. Primary drawback are that compared to traditional converters, they require stronger semiconductor switches. The cost of the system could grow even if employing switches with lesser rating may help to offset the cost rise to some extent. As we utilise more technologies, the likelihood of failure will increase. Switches with lesser voltage ratings can also be used in a multi-level converter, However, a gate driving circuit is unique to each switch [12]. The most popular among multilevel inverter topologies that have been documented are cascaded H bridges inverter have distinct dc souces (capacitor clamped), diode-clamped (neutral clamped), and flying-capacitors. Furthermore, several multilayer converter applications deal with service border for clean energies system, AC gearbox infrastructure (FACTS), traction initiative schemes [13],[14]. The multi-level inverter is a highly recommended alternative for medium to high voltage applications. The electrical grid can incorporate non-conventional energy thanks to multi-level inverters (MLI) [15],[16]. Three configurations exist for MLI:

- Multilevel inverter with diode clamping
- Flying-capacitor (FC) multilevel inverter
- Cascaded H-bridge (CHB) multilevel inverter

Currently, the CHB configuration is widely used due to its simplicity. The H-bridge cascade topology allows for the attainment of any desired number of voltage levels.

II. MATERIALS AND METHOD

These days, hybrid inverters in cascaded form are being explored because of their precision in producing a range of voltage levels with fewer transistors or switches. The following succinctly describes the primary advantages for suggested HMLI topology, which produces staircase voltage output level with a minimal count of switches. The main contribution of the proposed topology is summed up as follows:

I. Favourable aspects of packed U Cell (PUC) MLI and H-bridge type MLI are combined in the suggested topology. The H-bridge type MLI can create greater voltage levels with fewer components and less overall voltage stress because to this hybridization.

II. H-Bridge and Packed U Cell inverter are interconnected in a cascading manner.

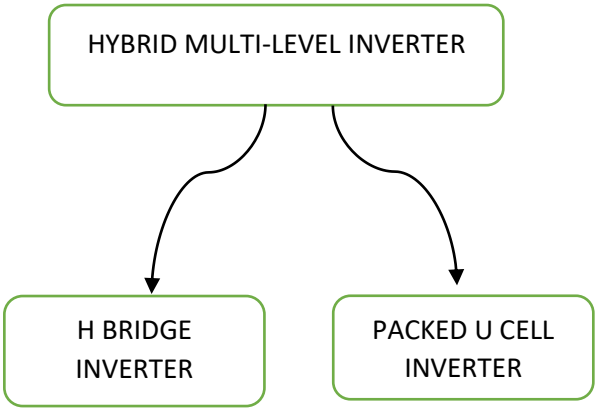


Fig.1

A. H Bridge inverter

H Bridge is consisting of four switches from Q_a to Q_d. The given semi-conductor switches are high voltage low frequency switches and generate three level output which is shown in Fig 4(a) and its output is input to Packed U Cell inverter.

Table 1.1 3-level H-bridge switching states

Switching states				Output voltage
Qa	Qb	Qc	Qd	
1	0	1	0	+Vdc
0	1	1	0	0
0	1	0	1	--Vdc

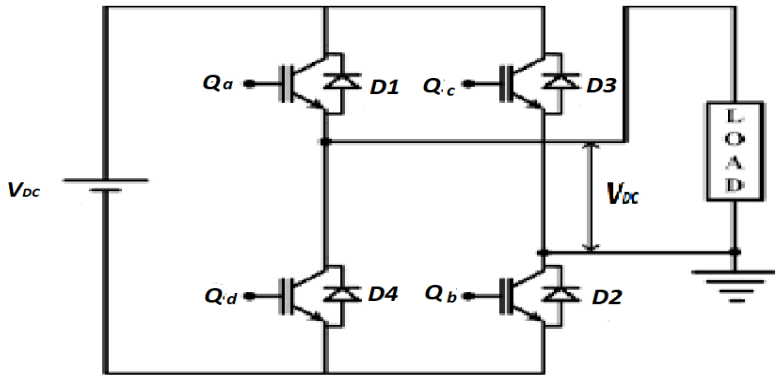


Fig. 2 H Bridge inverter

B. *Packed U Cell (PUC) inverter*

The PUC is composed of six switches from Q_1 to Q_6 having two voltage sources D_{dc} and $V_{dc}/2$. Switches are high voltage high frequency switches. This inverter generates 7 level output which given in Fig. 4(b), it takes input from H Bridge. There are 11 levels in the output that is produced: $+5/2V_{dc}$, $+2V_{dc}$, $+3/2V_{dc}$, $+1V_{dc}$, $+1/2V_{dc}$, $0V_{dc}$, $-5/2V_{dc}$, $-2V_{dc}$, $-3/2V_{dc}$, $-1V_{dc}$ and $-1/2V_{dc}$.

Table 1.2 7-level Packed U Cell switch states

Mode	Q1	Q2	Q3	Q4	Q5	Q6	Vdc
1	1	0	0	1	0	1	+3/2Vdc
2	0	1	0	1	1	0	+Vdc
3	1	0	1	0	1	0	+1/2 Vdc
4	1	0	1	0	0	1	0
5	0	1	0	1	0	1	-1/2Vdc
6	1	0	1	0	0	1	-Vdc
7	0	1	1	0	1	0	-3/2Vdc

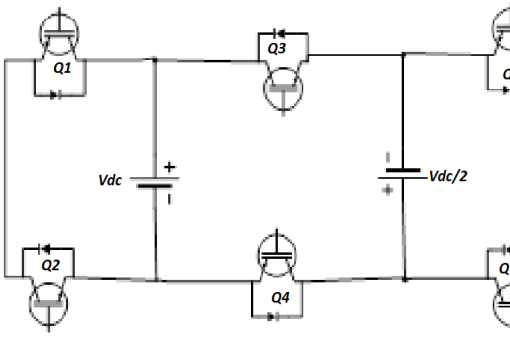


Fig.3 Packed U Cell (PUC) inverter

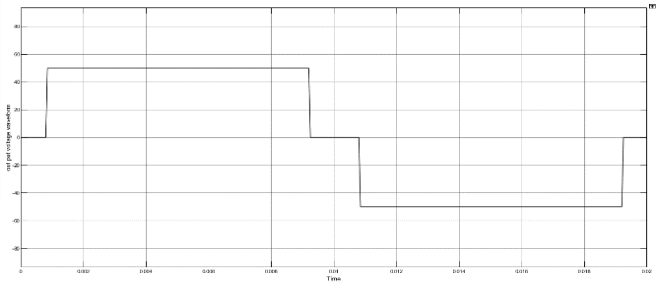


Fig.4(a) Single H Bridge Wave

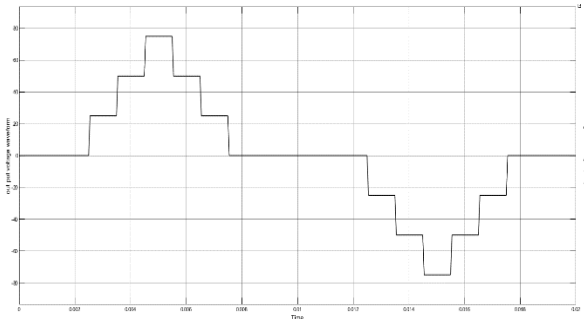


Fig.4(b) Packed U Cell Wave.

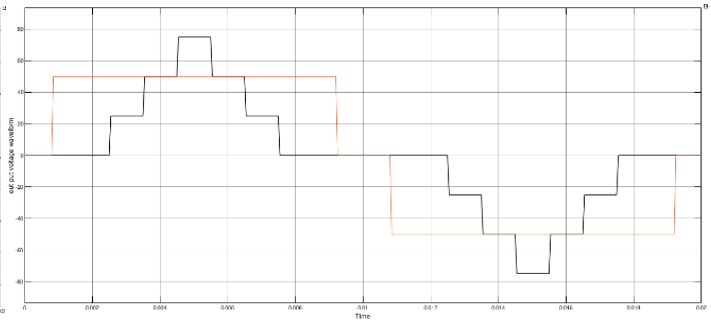


Fig. 4(a&b) Combined wave of H.bridge & Packed U Cell

C. The Suggested HMLIs Design

The inverter architecture is represented in Fig. 4(c) and consists of a PUC connected in series with a single H-bridge converter. This configuration is similar to the topology discussed in the section before it. However, this design generates an 11-level output waveform, a voltage source (Vdc) and 4 semiconductor switches (Qa to Qd) make up an H-bridge. The PUC inverter, on the other hand, has 6 semiconductor switches (Q1 through Q6) and two voltage sources Vdc and Vdc/2.

Table 1.3 11-levels HMLI inverter mood of switching

Mode	Qa	Qc	Qb	Qd	Q1	Q2	Q3	Q4	Q5	Q6	Vo
1	1	1	0	0	1	0	0	1	1	0	+5/2Vdc
2	1	1	0	0	1	0	0	1	0	1	+2Vdc
3	1	1	0	0	0	1	0	1	1	0	+3/2Vdc
4	1	1	0	0	0	1	0	1	0	1	+1Vdc
5	1	1	0	0	1	0	1	0	0	1	+1/2Vdc
6	1	1	0	0	0	1	1	0	1	0	0
7	0	0	1	1	0	1	0	1	1	0	-1/2Vdc
8	0	0	1	1	1	0	1	0	1	0	-1Vdc
9	0	0	1	1	1	0	1	0	0	1	-3/2Vdc
10	0	0	1	1	0	1	1	0	1	0	-2Vdc
11	0	0	1	1	0	1	1	0	0	1	-5/2Vdc

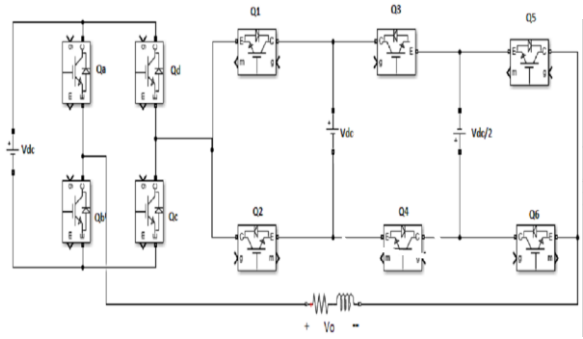


Fig. 4(c) Suggested HMLI Design

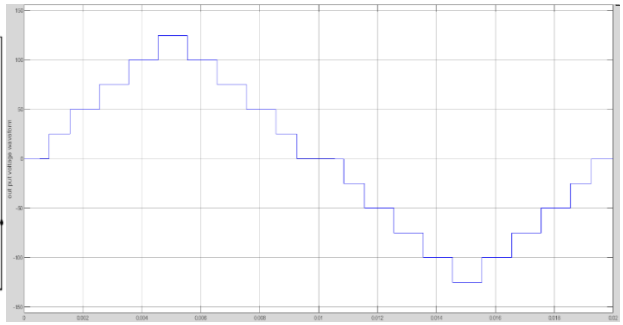


Fig. 4(d) HMLI output waveform

Math formulas

Eq. can be used to calculate the HMLI inverter's output voltage. (1):

$$V_{(Out)} = V_{(H\text{-}Bridge)} + V_{(PUC)} \quad (1)$$

Math design to suggested Hybrid Multiple level inverter are characterized by the subsequent set of equalities: (2)–(4):

$$di/dt = 1/L(S_xV_{c1} + S_yV_{c2} \pm S_zV_{dc}) \quad (2)$$

$$dV_{c1}/dt = S_{xi}/C_1 \quad (3)$$

$$dvc2/dt = S_{yi}/C_2 \quad (4)$$

The following set of formulas can be used to model the proposed HMLI converter mathematically. (5)–(7):

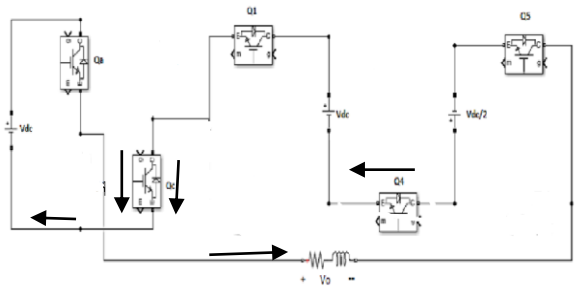
$$S_x = Q_1Q_4 - Q_2Q_3 \quad (5)$$

$$S_y = Q_4Q_5 - Q_3Q_6 \quad (6)$$

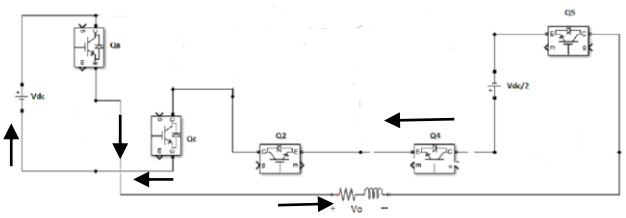
$$S_z = Q_aQ_d - Q_bQ_c \quad (7)$$

IV MODES OF OPERATİON FOR HYBRİD MULTİ-LEVEL İNVERTERS

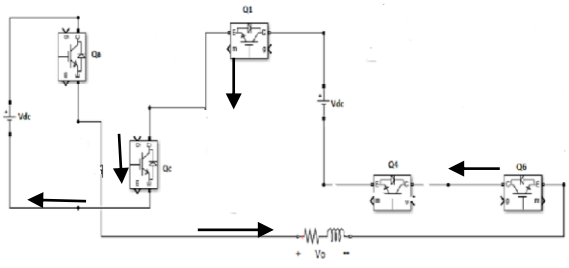
MODE: I Vo=+5/2V_{dc}



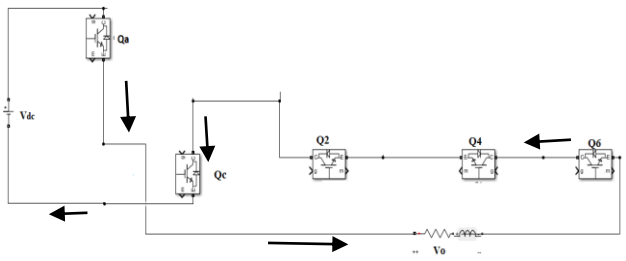
MODE: III V_o = +3/2V_{dc}



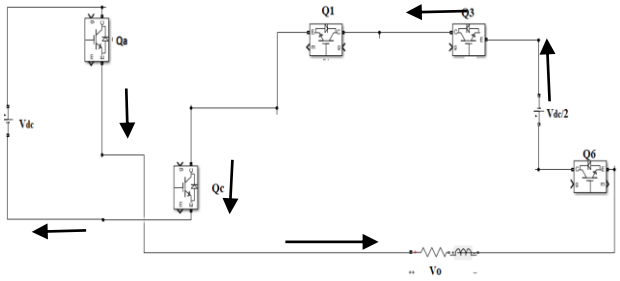
MODE: II V_0 = +2V_{dc}



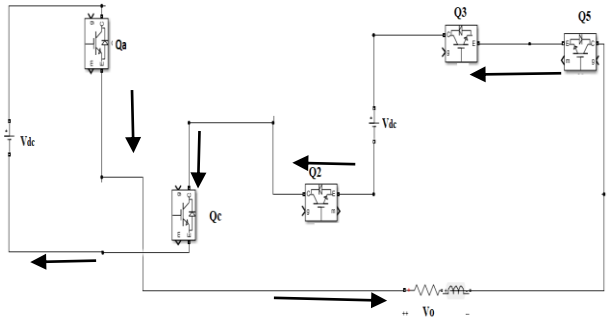
MODE: IV V0 = + 1V_{dc}



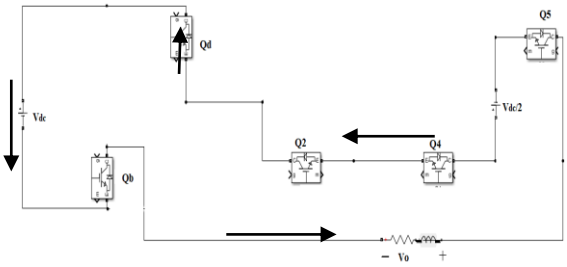
MODE: V V_o = + 1/2V_{dc}



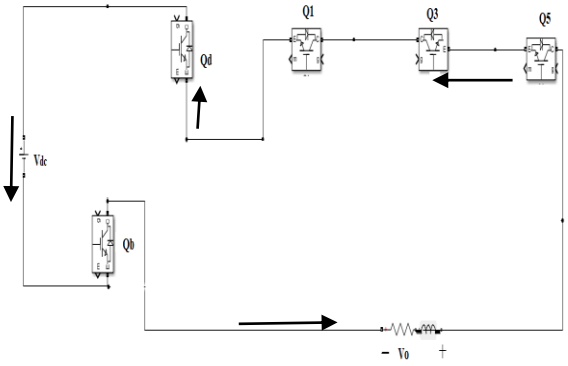
MODE: VI V_o = 0V



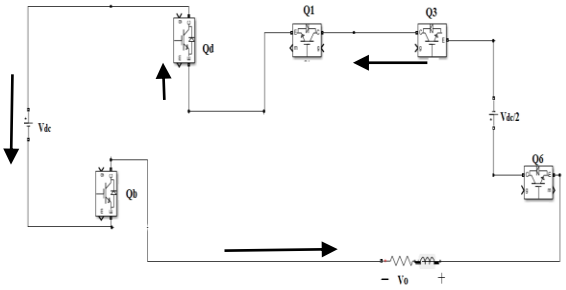
MODE: VII V_o= -1/2V_{dc}



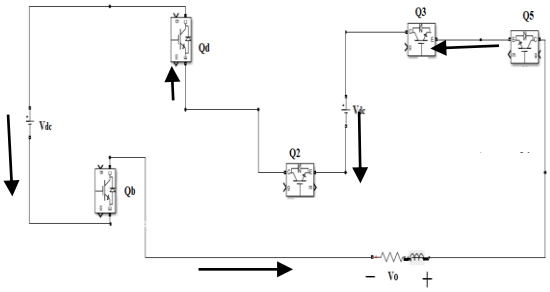
MODE: VIII V0 = -V_{dc}



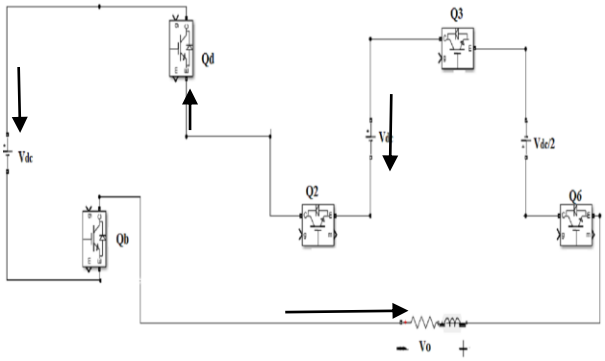
MODE: IX V_o = -3/2V_{dc}



MODE: X V_0= -2V_{dc}



MODE: XI V_0= -5/2V_{dc}



III. RESULTS

Suggested scheme has hybrid multiple level inverter, as depicted in figure 4(c), was simulated in the MATLAB/Simulink environment and the system component values are given in Table 1.4. This simulation yielded the best overall performance and effectiveness ratings. The HMLI model architecture creates 11 levels of output voltage by connecting the inverter's H-Bridge topology in series with a 7-level suggested topology called Pack-U Cell (PUC), as illustrated in fig. 4(c). With an anticipated efficiency of above 97.5%, this specific type of HMLI design is meant for medium voltage high power applications. The meticulous analysis of component values by appropriate modelling of stringent requirements. Fig. 6(i to iii) displays outcomes of the hybrid multiple level inverter output amplitude voltage simulations. Fig. 6(i) displays the voltage output of the H bridge unit. Fig. 6(ii) displays the output voltage of the Pack- U-Cell(PUC) and Fig. 6(iii) displays the voltage output of the HMLI. The outcomes were gotten with the modulation index of 1.

Table 1.4: Parameter of Inverter System.

Parameter	Values
Voltage of DC Bus	125v,100v,75v,50V,25v
Cell Carrier Frequency of H Bridge	50 Hz
Carrier Frequency of PUC	5KHz
Load	R= 20 ohms, L=8mH

Technique of Modulation

Inverters use a type of modulation called SPW Modulation or sinusoidal pulse width modulation. When an inverter with circuits for switching from a DC input produces a number of square voltage pulses each half cycle, the result is a sine wave. Sinusoidal PWM is a very well-known method of controlling AC engines. This method uses convergence targets to regulate the substituting objectives of the triangle-shaped wave carrier that is modified by the sine wave is used to power the inverter's electrical components. Despite not being able to use the inverter's entire supply power, this method is nevertheless widely used and results in severe harmonic distortion in the supply because of the PWM flipping characteristics' irregular nature. A few pulses are produced per half cycle with this modulation. For that portion of the period, the pulse width is equal to similar amplitudes of a sine waveform due to the fact that pulses close to the partial cycle extremes are invariably thinner from those near to its Centre as shown in Fig.6. As we alter the effective output, all pulses width is varied while keeping sine wave proportionality. Modulation index M can found by comparing the carrier frequency f_c with the reference frequency f_{ref} as indicated in the equation below.

$$M=f_c/f_{ref}$$

In packed u cell we employed POD carrier based PWM to generate necessary gating signal for power switches. The carriers signal that is above and below the reference line in this PWM method, which is based upon the POD principle, have the same amplitude and frequency. Carriers above and below reference line, however, are 180 degrees out of phase. Fig.5 shows the PWM waveform for the Packed U Cell module using the POD carrier-based approach.

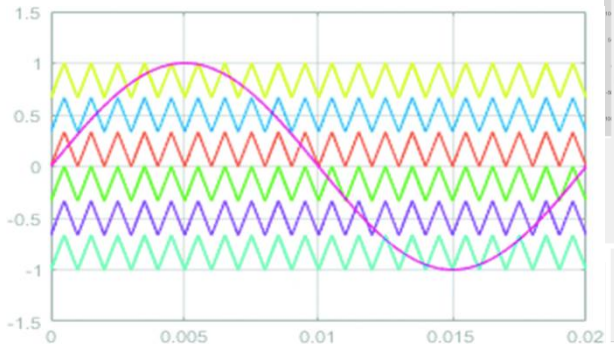


Fig.5 7 level shift-carrier Based POD-PWM technique

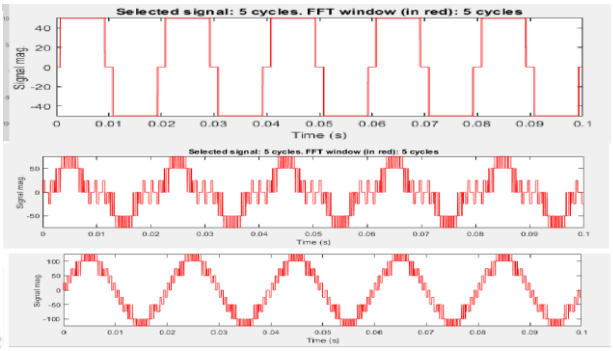


Fig.6 Waveform of the eleven-levels HMLI output at M=1
(i) H bridge wave output **(ii)** Packed U Cell output wave
(iii) HMLI output waveform

The HMLI model architecture creates 11 levels of output voltage by connecting the inverter's H-Bridge topology in series with a 7-level suggested topology called Pack-U Cell (PUC), as illustrated in fig. 6(iii). With an anticipated efficiency of above 98.5%, this specific type of HMLI design is meant for medium voltage high power applications. The meticulous analysis of component values by appropriate modelling of stringent requirements. Fig. 6(i to iii) displays outcomes of the hybrid multiple level inverter output amplitude voltage simulations. Fig.6(i) displays the voltage output of the H bridge unit. Fig.6(ii) displays the output voltage of the Pack- U-Cell(PUC) and Fig.6(iii) displays the voltage output of the HMLI. Fig.7 shows THD for the hybrid multiple level output at M=1. Fig.4C circuit is simulated with M=1, and total HMLI inverter's Total Harmonics Distortion values are designed for V(ab), V(bo), and the output V(o). The PUC module at M=1 greatly lowers harmonic distortion and generates an eleven-level output waveform by eliminating the third-order harmonic component. This filtering effect lowers THD and improves waveform quality by lowering harmonic output voltage. the current total harmonic distortion for modulation indice of M=1 is displayed in Fig.8 In the meantime, the current waves are displayed in accordance with these modulation indices in Figs. 4.11(a). Additionally, the current THD of the modulation indices is shown in Figs. 4.11(b), that are attached below

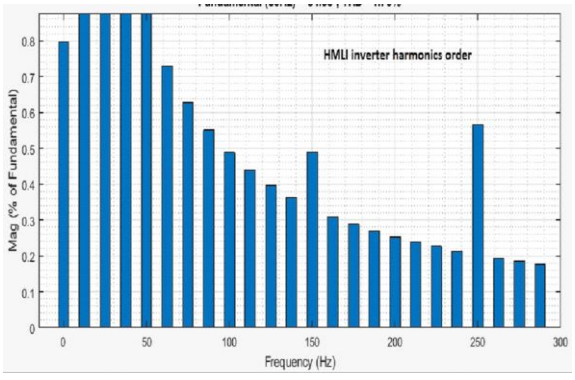


Fig.7 Total Harmonics Distortion (THD) using Fast Fourier Transform at M =1

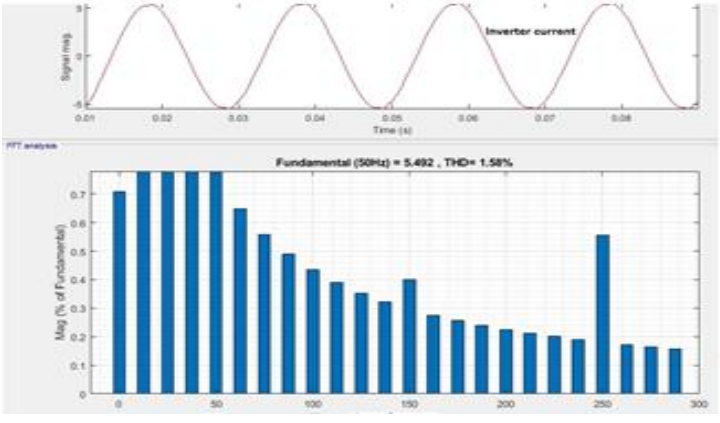


Fig.8 THD and waveform of Current at M= 1
(a) Waveform of Current
(**b**) Total Harmonic Distortion of Current

The current at the converter's yield across RL loads for a range of modulation indices is shown in Fig.9.

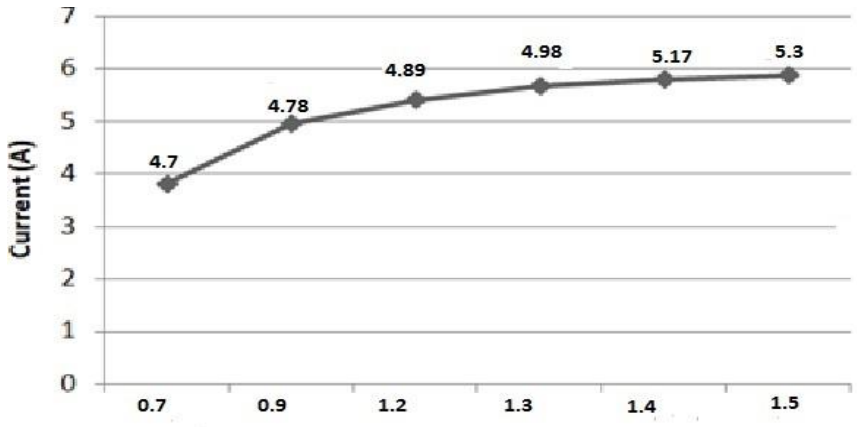


Fig.9 modulation indices values for Current (A).

IV. DISCUSSION

The HMLI topology has some benefits over the prior hybrid inverters in table 4.1 when compared with the same parameter. These comprise a lower number of things/switches, as tab.1.5 illustrates.

Table. 1.5: Parts of various converters.

Inverter	Active switch	Diode	Dc-link capacitor
NPC	8	4	2
HNPC with H-Bridge	10	2	3
HNPC with cascaded module	12	2	4
Proposed HMLI inverter	10	-	-

Four energetic switches, located inside the module's outer leg and subject to low voltage strain, are used in the HMLI design. Because of this, those switches run at high frequencies in order to minimise the needed inductor size and lessen contemporary ripple.

Table 1.6 voltage stress on switches & diode devices

Semiconductor deice	Voltage Stress	
	Active Switches	Diode
Half bridge NPC	E/2	E/2
Half bridge	E/2	-
PUC module center cell	E	-
PUC module outer cell	E/2 & E	-
H-Bridge	E	-

Table 1.7 displays the inverter's current total harmonic distortion (THD) at various energy scores. The desk almost entirely demonstrates how the well-known HMLI reduces modern THD in comparison to current hybrid inverter designs. This presents a comparison between the relevant hybrid and NPC inverter topologies and the existing general harmonic distortion (THD) for the proposed HMLI architecture over a variety of energy ratings. The results actually demonstrate that, in comparison to the relevant hybrid inverter topologies, the recommended inverter exhibits a lower THD.

Table. 1.7 Total Harmonics Distortion of current of HMLI operate at numerous power usage.

Inverter	Power rating		
	25 %	50%	100 %
NPC	5.31	2.83	1.38
HNPC with H-Bridge	6.71	3.43	1.73
HNPC with cascaded module	6.59	3.39	1.71
Proposed HMLI	6.57	3.35	1.69

V. CONCLUSION

The hybrid multiple level inverter architecture, specifically created for the programmed specially operating in the medium voltage range, has been simulated at various modulation index values. According to IEEE (519) criteria, the results show that the HMLI topology creates an output voltage with a maximum of eleven levels and lower voltage harmonic distortion as well as reduced generalized harmonic distortion (THD) of the current. Additionally, when compared to related hybrid multi-level inverter new topologies and NPC, the HMLI topology boasts a smaller object count while maintaining reduced THD and higher performance. The corresponding suggested HMLI model can generate yield voltage having 13 level by converting one of the inverter's DC sources. Additionally, this might reduce THD and enhance the HMLI's normal efficiency. In the future, the suggested study can be extended to a three-phase device configuration, which will enable the examination of innovative modulation and control techniques for this specific device.

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