Uluslararası İleri Doğa Bilimleri ve Mühendislik Araştırmaları Dergisi
Sayı 8, S. 358-368, 9, 2024

Araştırma Makalesi

IJANSER
https://as-proceeding.com/index.php/ijanser
ISSN:2980-0811

International Journal of Advanced Natural Sciences and Engineering Researches
Volume 8, pp. 358-368, 9, 2024

Research Article

Systematic Control Approach to Hybrid Inverter Topology for Higher Applications

Engr. Muhammad Uzair Shah[1] and Dr. Ajmal Farooq[2]

[1]*Department of Electrical Engineering,UET Mardan ,Mardan, Pakistan*
engruzairshah95@gmail.com
[2]*Department of Electrical Engineering , UET Mardan, Mardan, Pakistan*

(Received: 20 October 2024, Accepted: 27 October 2024)

(4th International Conference on Engineering, Natural and Social Sciences ICENSOS 2024, 22-23 October 2024)

ATIF/REFERENCE: Shah, M. U. & Farooq, A. (2024). Systematic Control Approach to Hybrid Inverter Topology for Higher Applications, *International Journal of Advanced Natural Sciences and Engineering Researches*, 8(9), 358-368.

Abstract- This paper proposed single phase-controlled Grid-connected hybrid inverter for higher power applications. The circuit is comprised of the series arrangement of T type three level inverter with active power filter of five level cascaded converter module. The level shift Pulse width modulation strategy is applied with low level complexity. The capacitor's voltages in cascaded converter module are balanced. Theoretically, the circuit is analyzed and gain Total harmonic distortion of 2.48%. The number of components used is less than as compared with the existing topologies. Moreover, the circuit complexity is reduced, the efficiency is increased by reducing stresses of voltages and current across the switches.

Keywords—Inverters, Hybrid Inverters, HMLI, HMLI-7.

I. INTRODUCTION

Renewable-energy-sources are getting attention due increase in demand of energy. The conventional energy sources have bad impact on the environment like air pollution due to diesel and coal generators, water pollution because of nuclear wastes. Renewable energy sources are environmentally friendly and available in abundance [1-4]. Solar energy is the most famous in renewable because sunlight is available in most places on earth. Perovskite based solar panels getting more attention due to cost effect and more efficient [5].

To harness the solar energy, first it should be converted from DC to AC, for which an inverter is needed. Conventional inverters have been used for decades and still used in the industry nowadays. Single phase inverters have two types half bridge and full bridge which gives ±Vdc/2 and ±Vdc. The conventional inverters are having less components used, therefore less energy loss across the components which make it more efficient. However, due to the high rate of changing current (di/dt) and rate of change changing voltage (dv/dt) generates the harmonics which leads to have heating effects, iron loss increases and decrease efficiency. The output of the inverter is having all the harmonics in which third harmonics is predominant. Moreover, the size of the inverter is increased because of bulky inductors. The Total Harmonics Distortion (THD) can be reduced by using Pulse Width Modulation (PWM) technique and the size of the inductors can be reduced which make it cost effective. The usage of the inverters is limited to the low and medium voltage range because for high voltage range, it requires high voltage and high current rating of switches which are very costly or either not available. Additionally, the voltage stresses on each switch are very high [6-9].

To deal with all these problems associated with conventional PWM inverters, Multi-Level Inverters (MLIs) got more attention. The heat losses in the MLIs are greater as the number of switches increases but overall, the THD of the inverter is highly reduce. The major plus point of the MLIs over two or three level inverters is that it gives a high-quality output at low switching frequency. The higher the number of levels, the output waveform will be more sinusoidal and moreover, the higher will be the quality of the output and reduces the output inductor size. Additionally, the voltage stresses on the switches are also reduced. However, the control topology and the circuitry of the MLIs are getting more complex and cost and size is also increased [10].

Three basic MLI topologies which are used in industry are: Neutral Point Clamped (NPCMLI) or Diode Clamped (DCMLI), Flying Capacitor (FCMLI) and Cascaded H-Bridge (CHBMLI). The FCMLI and CHBMLI are introduced in the late 1960s and DCMLI has been initiated in 1970s. however, these MLIs are used for low power applications. In 1980s, the DCMLI and CHBMLI were evolved for medium voltage applications and in 1990 the DCMLI were made capable to handle medium range voltages [11]. Furthermore, in some topologies like FC and NPC, DC-link capacitors are added to provide different levels that are connected to switches which operate in a systematic manner to deliver the power to the load. However, the number of switches increases with as increase in levels due to achieve high voltages but the increasing number of switches leads to the losses in switching and also increase the complexity of the circuit which adversely affect the efficiency and reliability. All these MLIs requires isolated DC sources which is made up from PV panels, batteries or by using isolated transformers and then rectify the AC to DC. On the other hand, applying any of the above suggestions, the inverter will get bulky in size and also get costly. Additionally, the number of levels increased in MLIs, the imbalance of voltage across DC-Link capacitors also increased [12].

In this paper Hybrid Multi-Level Inverter 7 (HMLI-7) is proposed which is the combination of two cascaded converters namely T-Type and five level Cascaded Converter module (CCM-5). The HMLI-7 which is using less components and offers high quality output with increased efficiency. The topology is operated on lower frequency. The modulation technique which is used here in CCM-5 is Phase-Opposition-Disposition Pulse-width- modulation (PODPWM) technique.

II. PROPOSED SYSTEM

A. HMLI-7 Technique and Working

The proposed circuit of single phase voltage source inverter (VSI) Hybrid Multi-Level Inverter (HMLI) is based on the series configuration of three-level T-Type converter (TTC-3) and a five-level cascaded converter module (CCM-5). TTC-3 is composed of 4 switches (S_1,S_2,S_3,S_4) and two isolated sources each having E voltage across it. The CCM-5 consists of six switches ($S_x\bar{S}_x$,$S_y\bar{S}_y$,$S_z\bar{S}_z$) and two isolated sources having voltage $E_1 = E_2 = E$ across it as shown in figure 1.1. The DC sources are present in figure 1.1 is only for better understanding the working of the circuit, later on, the sources will be replaced with capacitors.

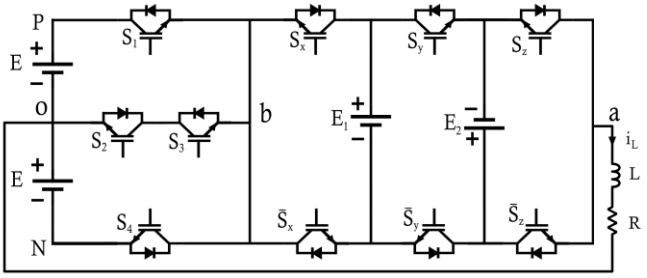

Fig. 2.1. Hybrid Muti-Level Inverter seven level topology diagram

The output of the TTC-3 is ±E and zero and operated at fundamental frequency which is 50Hz. The TTC-3 is shown in figure 1.2 where S_2 and S_3 are connected with o and b. The "o" is common point while b is the output of the converter. S_2 and S_3 can be connected either in common collecter configuration or in common emmiter configuration. The common emmiter aquire additional isolated drive which sums upto three isolated drive voltage supply to operate the TTC-3. That is why, common collector configuration is used here. Switches S_1,S_2 and S_3,S_4 are complemantory switches which are operating in opposite. To understand the operation of the TTC-3, the output of the converter will be +E when S_1 is switched on and -E when S_4 is switched on. The voltage stresses on S_1 and S_4 are maximum upto +2E. The output voltage will be zero when S_2 and S_3 are switched on and the voltage stress on these two switches are +E. The switching states are given in Table 1.1.

Table. 2.1. T Type three level converter switching states

STATE	S_1	S_2	S_3	S_4	V_{out}
P	ON	ON	OFF	OFF	+E
0	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	-E

The CCM-5 is the combination of two DC sources and six switches as shown in figure 2.2. The voltages of the dc sources are $E_1 = E_2 = V$. Table show the different output voltages of the given figure 2.2. The voltages that are generated by the CCM-5 is 0, ±V, ±2V and will be quasi square wave. The Source voltages of the DC sources that is feed to the CCM-5 will be the half of the voltage of the DC sources of the TTC-3. The number switches are increased with respect to the number of switches that are used in TTC-3, so, the voltage stress on each switch will be divided and the net voltage stress on each switch be less as compare to that of the TTC-3 and the heat dissipation will be minimum.

Table. 2.2. Cascaded Converter Module five level switching states

STATES	S_x	S_y	S_z	V_{ba}
1	ON	OFF	OFF	0
2	ON	OFF	ON	0
3	ON	ON	OFF	-V
4	ON	ON	ON	+V
5	OFF	OFF	OFF	-V
6	OFF	OFF	ON	+V
7	OFF	ON	OFF	-2V
8	OFF	ON	ON	+2V

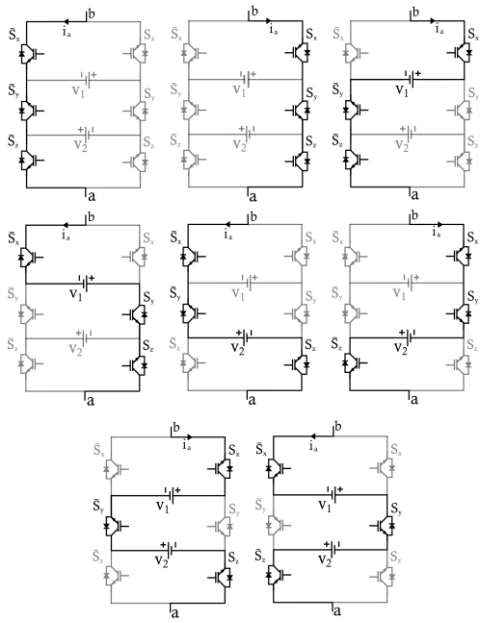

Fig. 2.2. Switching and conducting paths of CCM-5.

The output of the TTC-3, CCM-5 and HMLI-7 shown in figure 2.3 (a), (b) and (c). As given in the figure2.3 (c), the quasi-square wave is generated which consist of seven levels and having ±3E, ±2E, ±E and 0 voltages. The more output voltage levels, the less will be the dv/dt and di/dt. So, the output of the HMLI-7 is getting more sinusoidal and filters that are used on the output will be of less value and the size will also be reduced. The switching states of the HMLI-7 is show in table. Switches $\bar{S}_x$, $\bar{S}_y$ and $\bar{S}_z$ are operating in complementary of S_x, S_y, S_z.

Table. 2.3. All possible switching states of CMM-5 table

STATES	S_1	S_2	S_3	S_4	S_x	S_y	S_z	V_{oa}
1	OFF	ON	ON	OFF	ON	ON	ON	0
2	ON	OFF	OFF	OFF	ON	ON	ON	+E
3	OFF	OFF	OFF	ON	OFF	OFF	OFF	-E
4	ON	OFF	OFF	OFF	ON	ON	OFF	+2E
5	OFF	OFF	OFF	ON	OFF	OFF	ON	-2E
6	ON	OFF	OFF	OFF	OFF	ON	OFF	+3E
7	OFF	OFF	OFF	ON	ON	OFF	ON	-3E

B. HMLI-7 implementation

The efficiency of the circuit is dependant on the number of component used in the circuit. If the number of the component is increased, the efficiency will be decreased and vice versa. Similarly, the efficiency of the HMLI topologies or any other converter topologies can be improved by reducing the number of component used so that the switching losses is reduced. In HMLI-7, the switches of the TTC-3 is under high voltage stress. Moreover, if the swtiching frequency is increased, the TTC-3 losses will also increase and reduce the overall efficiency of the circuit. To reduce the switching loss, TTC-3 is operating at fundamental frequency which 50Hz. The high harmonics will be produced by the reducing the switching frequency which is mitigated by using active power filter (CCM-5). The proposed topology as shown in figure 2.4 is using four DC sources. Two sources are operating the H-bridge and other two are using in CCM-5.

The proposed topology is the series combination of three- level TTC-3 and five level cascaded converter module to make seven-level converter as depicted in figure 2.4. Five level converter is made of six switches and two DC-Linked capacitors C_1 and C_2. These capacitors are at first charged up to E_{C1} = E_{C2} = E. The fundamental frequency which is 50Hz is generated by TTC-3 converter having output of ±E

and 0. The CCM-5 act as a series active filter and generates five level output which are ±2E, ±E and 0. The combined operation of the TTC-3 and CCM-5 will generate voltage of seven level output.

The cascaded converter module in the HMLI-7 topology plays important role in the proposed topology as it assures of giving seven level output with minimum harmonic distortions. When the voltage of the DC-Link capacitors is balanced according to its reference, the five level output by the CCM-5 will be ensured by eight different switching states as shown in figure 2.2. In cascaded converter module, ±E and 0 has redundant switching states while for ±2E, the switching states are unique. The change in current only determines the change in ±2E.

The effect of the different states on the capacitors are shown in Tables 2.4 and 2.5. Table 2.4 is applicable when the current is flowing from “a” to “o”. The different states are shown in figure 2.4 where DC sources were changed with capacitor as in CCM-5. In States 1 and 2, there is no effect on the capacitors however, in state 3, the capacitor C_1 is charging. Similarly, in state 4, C_1 is discharging and same is applied on the other states.

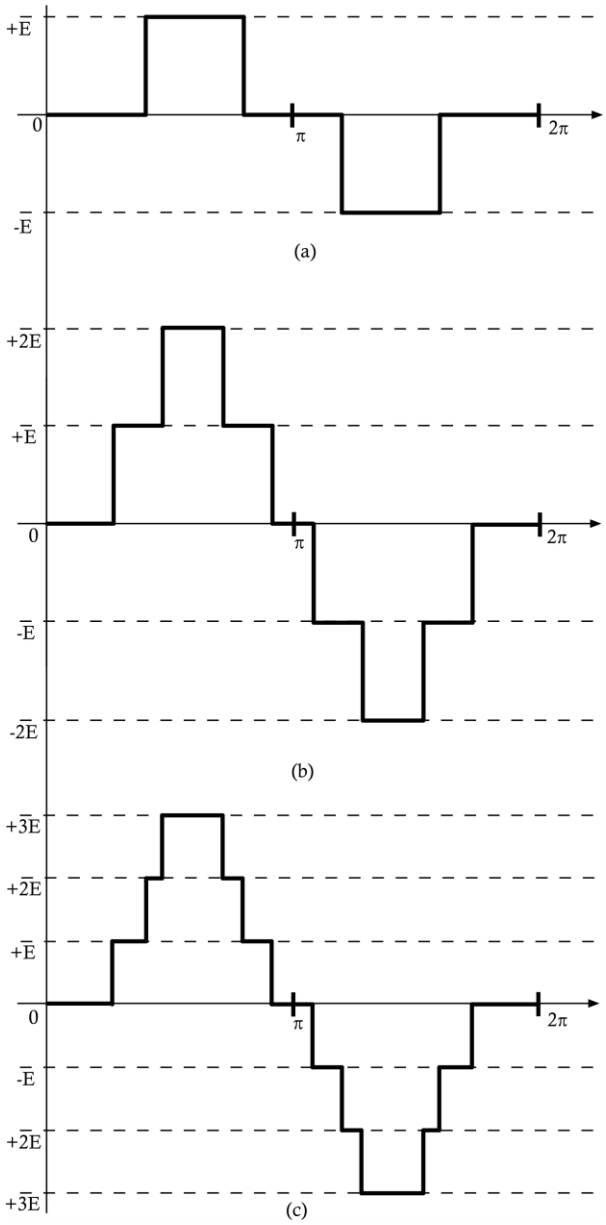

Fig. 2.3. Output Voltages waveforms (a) three level TTC-3 voltage output (b) Five level CCM-5 output voltages (c) Seven level HMLI-7 output voltages

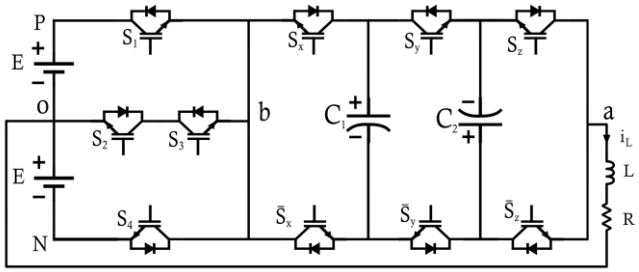

Fig. 2.4. Hybrid Muti-Level Inverter seven level topology diagram

Table 2.5 when the current is moving from “o” to “a”, the current is now moving in opposite direction, so, the effect of charging and discharging of the capacitors are also reversed.

Table. 2.4. Effect of the Capacitors when current i_L is from a to o

STATES	C_1	C_2
STATE 3	CHARGE	BYPASS
STATE 4	DISCHARGE	BYPASS
STATE 5	BYPASS	CHARGE
STATE 6	BYPASS	DISCHARGE
STATE 7	CHARGE	CHARGE
STATE 8	DISCHARGE	DISCHARGE

Table. 2.5. Effect of the Capacitors when current i_L is from o to a

STATES	C_1	C_2
STATE 3	DISCHARGE	BYPASS
STATE 4	CHARGE	BYPASS
STATE 5	BYPASS	DISCHARGE
STATE 6	BYPASS	CHARGE
STATE 7	DISCHARGE	DISCHARGE
STATE 8	CHARGE	CHARGE

III. MODULATION SCHEME AND CONTROL STRATEGY

A. Modulation scheme

The modulation scheme for the HMLI-7 is base on two different stratagies. The first one is made for the TTC-3 which Pulse Width Modulation (PWM) based as shown in figure 3.1. Additionally, more precise the technique is vertical phase shift PWM. In this technique, the reference sine wave and two carrier waves (Cw_1, Cw_2). These two carrier waves are shifted vertically to modulate the sine reference. The technique is well suited for cascaded MLIs.

The modulation technique for cascaded converter module is based on four carrier waveforms that is shifted vertically and is know as phase opposition disposition technique (PODT). In PODT, the signals are inverted or in other words, shifted by 180^0 degrees. The signal through which modulation occurs is the difference of the output of the TTC-3 and fundamental sine wave which is shown in figure 3.2.

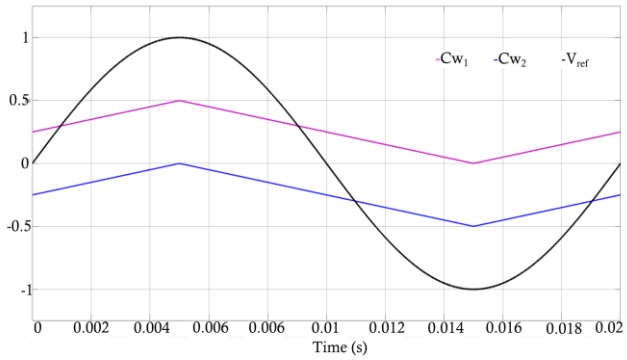

Fig. 3.1. TTC-3 waveforms

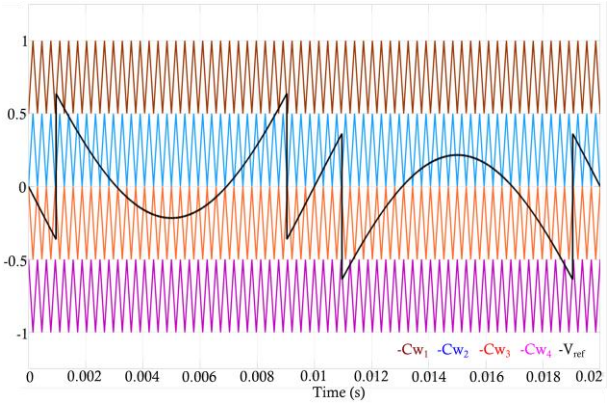

Fig. 3.2. Feed signal to CCM-5 with source vertical phase shift PWM.

B. Grid-Connected Mode Configuration & Controll

The grid connected HMLI-7 is shown in figure 3.3 with associated controller. Moreover, the current i_i is the current injected to grid from the inverter. The controller here is used to control the voltage magnitude and phase-shift of current i_i which in result delivers the active power to the grid while exchanging reactive power by HMLI-7.

The phase-Lock-Loop (PLL) is used to take the angle from the alternating current source v_{source} and measure it. The angle is then added to the grid voltage of the desired phase shift which is denoted by the symbol θ^*. Moreover, the angle θ^* is used to take reactive from the grid and exchange it with active power generated by the inverter. Thus, θ^* is responsible for making *the* power factor 0 and 1. For unity power factor, the angle θ^* should be 0 to ensure that the current is synchronized with v_{source}. To exchange reactive power, the power factor should be less than 1. For example, if the desired power factor is 0.5 then the angle $\theta^* = 60^o$. Then, the reference angle is feed to the sine block to produce a unit sine wave of desired phase shift. The unit sine is then multiplied by the maximum reference current I_{max}. I_{max} is the current which control the amount of power injected to the grid. The product is shown by i_i^* as reference current that is generated by the inverter. The unit current i_i^* is then compared with the actual current i_i, the error signal is feed to the proportional integral to minimize the steady state error. The reference voltage v_{ref} that is generated by the PI controller is then fed to the switches for modulation. The control strategy is used in [13]. The inductor L_f is used to smooth and control the current that is injected into the grid. Moreover, the inductor is also contributed in voltage regulation to make sure, the invertor output voltage is matched with the grid requirements.

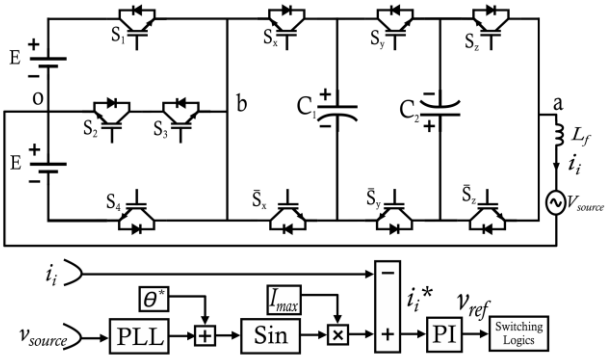

Fig. 3.3. HMLI-7 with control strategy

The proposed topology simulation is simulated in MATLAB 2021b. The HMLI-7 topology is observed in both stand alone and as well as grid-connected modes. The parameters are shown in table 3.1.

Table. 3.1. HMLI-7 Parameters

STATES	Values
DC-Link Capacitor	5000uF
CCM-5 carrier frequency	5KHz
Capacitor Voltage	160V
DC-bus Voltage	160V
Load	44ohm, 2.4mH

The gate signals that are given to the switches/IGBTs of the TTC-3 are given in figure 3.1. The three level signals will generate three levels +E, 0 and -E. The +E is from 0.001 to 0.009 and -E from 0.011 to 0.019. The 0V is in 0-0.001, 0.009-0.011 and 0.019-0.02.

The gate signals of the cascaded converter module are show in figure 3.2. The output waveforms for the TTC-3, CCM-5 and overall output is shown in figure 3.3. The output of figure 3.3(a) shows the output of the TTC-3 at frequency 5KHz, the inductance of the grid linked capacitor is 15mH, the initial voltage value for the capacitor is 160V and the sources that are connected to the TTC is having voltages of 160V each. The five-level generated by CCM-5 is depicted in figure 3.3(b)

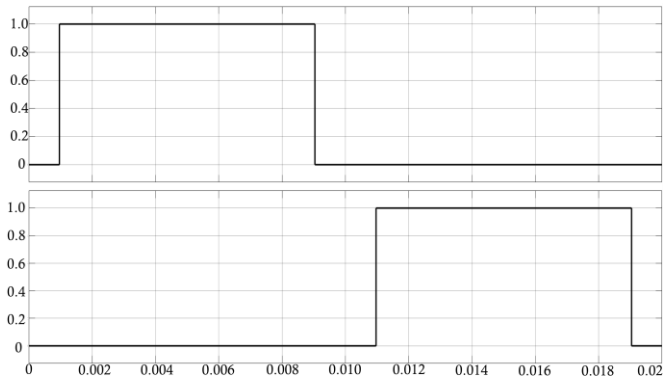

Fig. 3.1. Gate Signals for TTC-3 for switches S_1,S_4

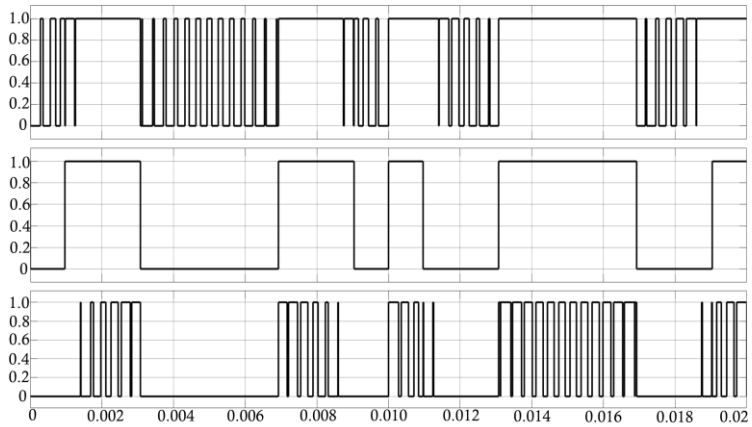

Fig. 3.2. Gate signals for CCM-5 switches S_x,S_y and S_z

where the maximum voltage that is generated is 320V. The overall output of the HMLI-7 is shown in figure 3.3(c). The quasi-square wave of the output voltage is having maximum voltage of 480V.

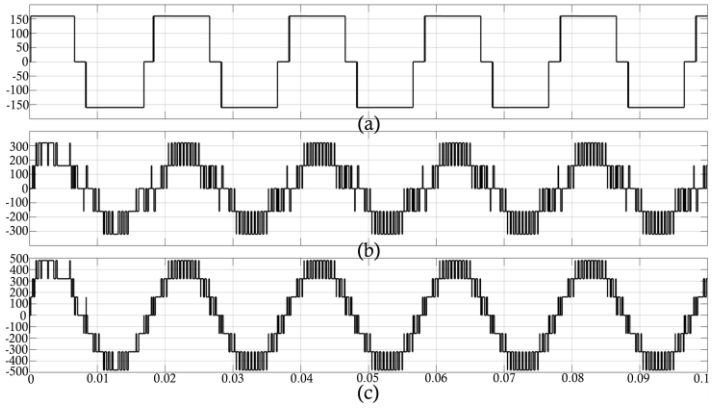

Fig. 3.3. Output waveforms without filters (a) TTC-3 (b) CCM-5 (c) HMLI-7

The output of the CCM-5 is generated according to the signal feed as shown in figure 3.2. To mitigate the harmonics that are present in the output of the TTC-3, CCM-5 act as an active power filter which generate negative of the harmonics. The negative voltage.

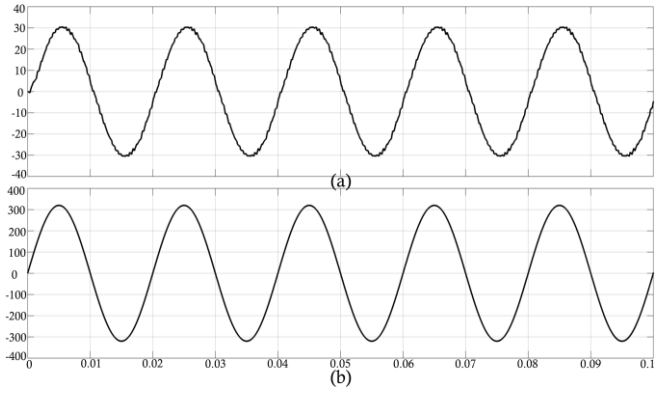

Fig. 3.4. Output waveforms after adding filters Grid connected (a) Current (b) Voltage

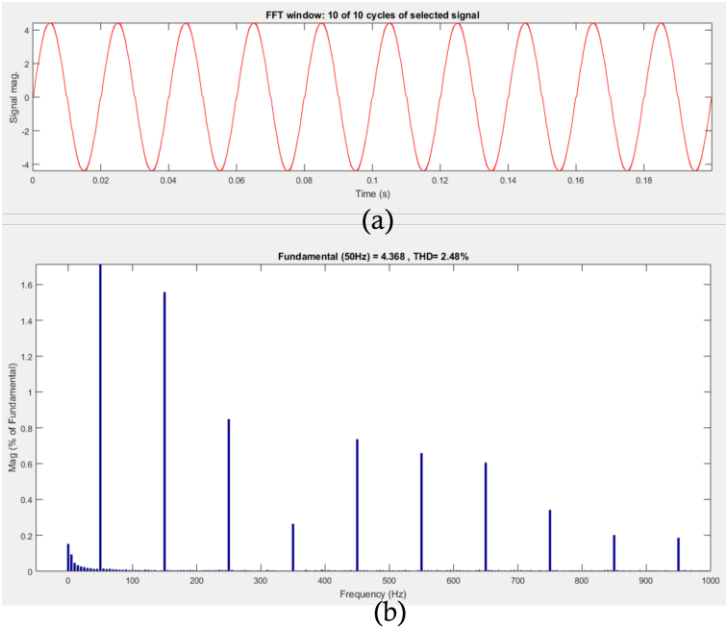

Fig. 3.5. THD of HMLI-7 when modulation index is 1.0

The output of the proposed HMLI-7 inverter is shown in figure 3.4 after filtration. In figure 3.5(a), the output current is analyzed, figure 3.5 (b) the Total Harmonic Distortion (THD) is 2.48% when the load is 44Ω and inductance is 2.4mH. In [17] seven level H bridge is being analyzed. The simulated THD of the seven-level H-bridge is 4.46%.

The THD on different modulation indexes are shown in table 3.2. The THD at modulation index at 0.9 is 4.45% and on modulation index 1.1 is 2.27%.

Table 3.2. THD at different modulation indexes.

Modulation Index	THD	LOAD
0.9	4.5%	44ohm, 2.4mH
1.0	2.48%	44ohm, 2.4mH
1.1	2.27%	44ohm, 2.4mH

C. Comparison based on components count of the proposed HMLI-7 with existing topologies

In Table 2.6, proposed methodology is compared with another topologies of having same levels based on components count. As per table, the proposed converter is using less components and have low level complexity. The proposed topology is straight forward and less complicated. The capacitor used in the proposed technique is two and no diode is used.

Table. 3.1. Analysis based on comparison of number of components count with existing topologies.

Inverter Type	DC Sources	Capac--itors	Clamp--ed Diode	Active Switchs	Total Parts Count	Control Compl--exity
[14] Cascaded H Bridge	3	0	0	12	15	Low
[15] Single phase seven level Grid connected inverter for PV system	1	3	8	6	18	Medium
[16] Hybrid 7 level inverter using low voltage devices & operation with single DC-link	2	3	0	12	17	Medium
Proposed HMLI-7 Topology	2	2	0	10	14	Low

IV. CONCLUSION

This paper presents the circuit configuration, control strategy and simulation for the proposed HMLI-7 topology. The topology is based on the series combination of special type of Neutral Point clamped topology named three level T-Type converter with series active filter of five level cascaded converter module. The simulation shows that the topology has several benefits like reducing switching losses, better efficiency, a smaller number of components counts and improved THD. The vertical shifted PWM based control strategy is very popular and suitable for the proposed topology. Proposed single phase HMLI-7 topology performance and effectiveness shows that the hybrid topology is validated through using simulation. The result of this paper shows that the new hybrid topology has been successfully simulated having high efficiency and lower THD at specific load when compared with existing topologies.

V. REFERENCES

[1] Bashir, Farrukh, and Savera Gull. "The Role of Renewable Energy in Mitigating Climate Change." *Available at SSRN 4833338* (2024).

[2] Elavarasan, Rajvikram Madurai, et al. "A comprehensive review on renewable energy development, challenges, and policies of leading Indian states with an international perspective." *Ieee Access* 8 (2020): 74432-74457.

[3] Martins, Florinda, et al. "Analysis of fossil fuel energy consumption and environmental impacts in European countries." *Energies* 12.6 (2019): 964.

[4] Panwar, N. L, S. C Kaushik, and Surendra Kothari. "Role of renewable energy sources in environmental protection: A review." *Renewable and sustainable energy reviews* 15.3 (2011): 1513-1524.

[5] Ito, Seigo. "Research Update: Overview of progress about efficiency and stability on perovskite solar cells." *APL Materials* 4.9 (2016).

[6] Bughneda, Ali, et al. "Review of multilevel inverters for PV energy system applications." *Energies* 14.6 (2021): 1585.

[7] Wang, Zhongjing, et al. "Design and validation of a 250-kW all-silicon carbide high-density three-level T-type inverter." *IEEE Journal of Emerging and Selected Topics in Power Electronics* 8.1 (2019): 578-588.

[8] Barah, Sushree Smrutimayee, and Sasmita Behera. "An optimize configuration of H-bridge multilevel inverter." *2021 1st International Conference on Power Electronics and Energy (ICPEE)*. IEEE, 2021.

[9] di Benedetto, Marco, et al. "Efficiency comparison of 2-level sic inverter and soft switching-snubber SiC inverter for electric motor drives." *Energies* 14.6 (2021): 1690.

[10] Mali, Rushikesh, et al. "Performance comparison of two level inverter with classical multilevel inverter topologies." *2019 IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT)*. IEEE, 2019.

[11] Mali, Rushikesh, et al. "Performance comparison of two level inverter with classical multilevel inverter topologies." *2019 IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT)*. IEEE, 2019.

[12] Naik, Banavath Shiva. *Investigation and Design of Capacitor-Based Multilevel Inverters*. Diss. National Institute of Technology Karnataka, Surathkal, 2022.

[13] Vahedi, Hani, Philippe-Alexandre Labbé, and Kamal Al-Haddad. "Sensor-less five-level packed U-cell (PUC5) inverter operating in stand-alone and grid-connected modes." *IEEE Transactions on Industrial Informatics* 12.1 (2015): 361-370.

[14] Atkar, Dipesh, et al. "Control of seven level cascaded H-Bridge inverter by hybrid SPWM technique." *2016 IEEE international conference on power electronics, drives and energy systems (PEDES)*. IEEE, 2016.

[15] Rahim, Nasrudin A., Krismadinata Chaniago, and Jeyraj Selvaraj. "Single-phase seven-level grid-connected inverter for photovoltaic system." *IEEE transactions on industrial electronics* 58.6 (2010): 2435-2443.

[16] Yadav, Apurv Kumar, et al. "A hybrid 7-level inverter using low-voltage devices and operation with single DC-link." *IEEE Transactions on Power Electronics* 34.10 (2019): 9844-9853.

[17] Yarlagadda, Anil Kumar, et al. "A modified seven level cascaded H bridge inverter." *2018 5th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON)*. IEEE, 2018.