Uluslararası İleri Doğa Bilimleri ve Mühendislik Araştırmaları Dergisi
Sayı 9, S. 129-137, 5, 2025

Araştırma Makalesi

IJANSER
https://as-proceeding.com/index.php/ijanser
ISSN:2980-0811

International Journal of Advanced Natural Sciences and Engineering Researches
Volume 9, pp. 129-137, 5, 2025

Research Article

Energy-Efficient Deep Learning through Memristive Neuromorphic Synapses: A Hardware Implementation Study

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(Received: 30 April 2025, Accepted: 07 May 2025)

(4th International Conference on Scientific and Innovative Sutdies ICSIS 2025, April 29-30, 2025)

ATIF/REFERENCE: Gökgöz, B. (2025). Energy-Efficient Deep Learning through Memristive Neuromorphic Synapses: A Hardware Implementation Study. *International Journal of Advanced Natural Sciences and Engineering Researches*, 9(5), 129-137.

Abstract- Advances in artificial intelligence and machine learning, especially in deep learning, have driven rapid adoption across various fields. However, the high computational demands and extensive data processing needs of these algorithms pose major energy efficiency challenges for traditional Von Neumann-based computing systems. These issues are compounded by the slowing scalability of semiconductor technology and the inefficiencies of parallel processing in multi-core architectures. To address these limitations, neuromorphic computing systems which unify memory and processing at the hardware level have emerged as a promising solution for energy efficient AI. Among their key components, memristive devices stand out by mimicking biological synaptic behavior with extremely low power consumption, allowing for physical representation of synaptic weights in neural networks. This study explores the hardware implementation of memristive synapses in deep neural networks. While memristive systems may have longer training times compared to software-based convolutional neural networks, they achieve competitive accuracy (up to 90%) using gradient descent optimization methods, all while consuming around 100,000 times less energy. This dramatic improvement in energy efficiency makes memristive technology a leading candidate for both current and future sustainable AI systems.

Keywords — AI Accelerators, Machine Learning, Memristors, Neuromorphic Computing, Synapses.

I. INTRODUCTION

The advent of contemporary information technologies has ushered in an era of exponential growth in artificial intelligence (AI), marked by paradigm-shifting innovations that continue to redefine computational capabilities. Within this landscape, machine learning (ML) and deep learning (DL) have emerged as cornerstone methodologies, distinguished by their robust accuracy, inherently scalable architectures, and dynamic adaptability attributes that have cemented their utility across an expansive array of scientific, industrial, and societal domains (Malhotra & Singh, 2023). Initially confined to theoretical research and experimental prototypes, these techniques have undergone a rapid transition toward real-world deployment, a shift propelled by synergistic advancements in algorithmic sophistication, the proliferation of high-performance computing (HPC) infrastructures, and the democratization of vast, annotated datasets.

Today, ML and DL frameworks constitute indispensable tools for addressing previously intractable problems, spanning applications from high-dimensional data mining and probabilistic predictive analytics to real-time computer vision, autonomous robotic systems, and semantic natural language processing

(NLP). Notably, the evolution of computational paradigms particularly the convergence of parallelized GPU architectures and distributed cloud computing has further potentiated the role of DL in revolutionizing NLP subfields. This is evidenced by transformative strides in neural machine translation (NMT), speaker-independent speech recognition, fine-grained image classification, and context-aware recommendation engines.

A seminal development in this trajectory has been the rise of large language models (LLMs), such as OpenAI's ChatGPT, which epitomize the culmination of years of research in transformer architectures, self-supervised learning, and massive-scale parameter optimization (Sarker, 2021). These models have not only achieved unprecedented benchmarks in linguistic tasks but also sparked interdisciplinary discourse on their ethical implications, energy efficiency, and societal integration highlighting AI's dual role as both a technological disruptor and a subject of critical scrutiny.

The accelerating trajectory of artificial intelligence (AI) research in recent years has elevated machine intelligence from a specialized discipline to a cornerstone of modern scientific inquiry, with algorithms such as artificial neural networks (ANNs), deep neural networks (DNNs), and machine learning (ML) frameworks now constituting indispensable tools across research domains. Nevertheless, a critical dichotomy persists between these biologically-inspired computational paradigms and the conventional von Neumann architecture that underpins modern computing systems (Gökgöz, Gül, et al., 2024). While von Neumann machines demonstrate exceptional proficiency in processing deterministic, rule-based operations, their architectural constraints render them fundamentally mismatched to the parallel, stochastic, and adaptive nature of neural computation (Sarpeshkar, 1998).

This incompatibility originates from first principle divergences in information processing mechanisms. The von Neumann paradigm enforces a rigid separation between processing units and memory hierarchies, incurring substantial energy and latency penalties through incessant data shuttling a phenomenon widely termed the "von Neumann bottleneck." In stark contrast, biological neural systems achieve remarkable energy-activity co-location, with synaptic plasticity enabling simultaneous memory retention and computation within unified neurobiological substrates. The efficiency gap is quantifiably stark: whereas modern supercomputers expend ~1 MW to execute complex AI workloads, the human brain accomplishes superior cognitive feats at a mere 10 W a five-order-of-magnitude advantage in energy efficiency (Zhu et al., 2020).

This architectural dichotomy is visually contextualized in Figure 1, where panel (a) depicts the linear, segregated memory-processor pipeline of sequential computing, while panel (b) illustrates the distributed, event-driven parallelism of neuromorphic architectures. Recognizing these limitations, the field has witnessed the rise of neuromorphic engineering a discipline seeking to transcend von Neumann constraints by co-integrating memory and computation through brain-inspired circuit design, spiking neural models, and memristive crossbar arrays. Such approaches aim to preserve the programmability of digital systems while achieving the energy proportionality and adaptive learning capabilities intrinsic to biological neural networks

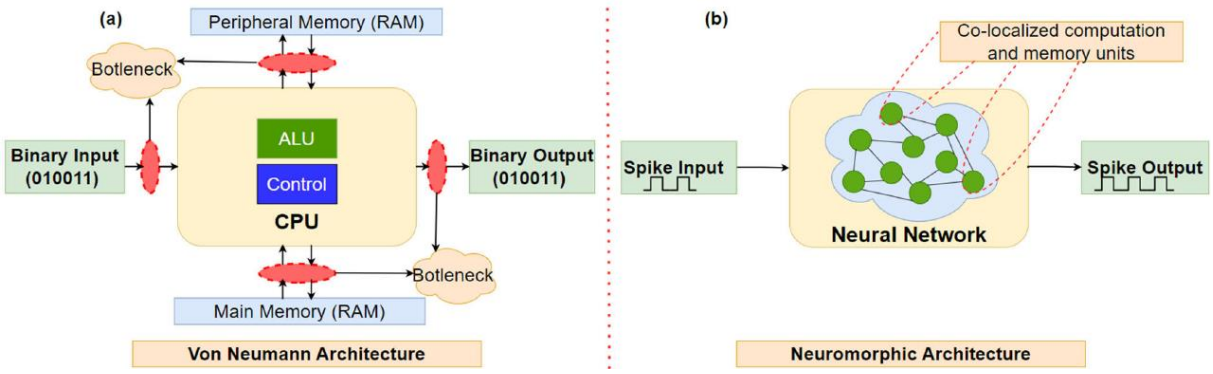

Figure 1. Panels (a) and (b) contrast von Neumann and neuromorphic architectures, highlighting divergent operational paradigms in computational logic, hardware organization, programmability, data flow, and temporal dynamics (Gökgöz, Aydın, et al., 2024).

Recent research has intensified focus on nanoscale semiconductor devices that mimic biological neural processing with high energy efficiency, addressing CMOS technology's scalability and power limitations. The brain's remarkable computational power stems from its massively parallel architecture, comprising hundreds of millions of interconnected neurons (Kuzum et al., 2013). Synapses the dynamic connections between neurons - enable not only signal transmission but also structural plasticity, forming the biological basis for learning, memory, and noise-tolerant adaptive computation.

To address this need, neuromorphic devices have emerged as artificial synapses capable of emulating biological synaptic plasticity. Memristors, as the core component, exhibit history-dependent conductivity modulation and non-volatile state retention properties that closely mirror biological synaptic weight adaptation. Their analog conductance tunability enables direct hardware implementation of synaptic learning mechanisms. This aligns with Hebbian plasticity principles, particularly Spike-Timing Dependent Plasticity (STDP), where synaptic efficacy depends on precise pre-/post-synaptic spike timing (Feldman, 2012). STDP has become fundamental for biologically-inspired learning algorithms in neuromorphic systems.

Consequently, memristors are prime candidates for hardware-level neuromorphic computing, offering native synaptic emulation, ultra-low power operation, and high-density integration.

II. ARTIFICIAL NEURON AND SYNAPSE

Artificial neurons and synapses are the fundamental building blocks of neuromorphic computing systems, which aim to emulate the structure and function of biological neural networks (Indiveri & Liu, 2015). An artificial neuron is a computational model that mimics the behavior of biological neurons by processing input signals, applying a transformation (often nonlinear), and generating an output signal (Indiveri & Liu, 2015; Mead, 1990). Artificial synapses, on the other hand, are responsible for modulating the strength of connections between neurons, analogous to synaptic weights in biological systems. These elements enable learning and memory functionalities in artificial networks by adjusting synaptic weights based on external stimuli and learning rules such as Hebbian learning or backpropagation. Recent advances in materials science, particularly in the development of memristive devices, have led to hardware implementations of artificial neurons and synapses, offering promising pathways toward energy-efficient and highly scalable neuromorphic processors (Chua, 1971; Prezioso et al., 2015).

Memristor-based neuromorphic systems offer an energy-efficient alternative for neural network implementation by enabling analog in-memory computation, circumventing von Neumann bottlenecks. These biologically-inspired architectures aim to replicate brain-like processing through interconnected neural models, combining memory and computation for event-driven, low-power (Chiu et al., 2023; Mead, 1990b). Unlike conventional AI accelerators focused solely on performance gains, true neuromorphic processors emphasize architectural biomimicry (Du et al., 2015).

Major tech firms (Google, IBM, NVIDIA, etc.) are developing specialized AI hardware including TPUs, FPGAs, and ASICs to optimize matrix operations fundamental to deep learning (Capra et al., 2020; Jouppi et al., 2017). Key challenges remain in balancing computational throughput, power efficiency, and production costs (Schuman et al., 2017), where memristive neuromorphic present a promising solution through native parallelism and synaptic emulation.

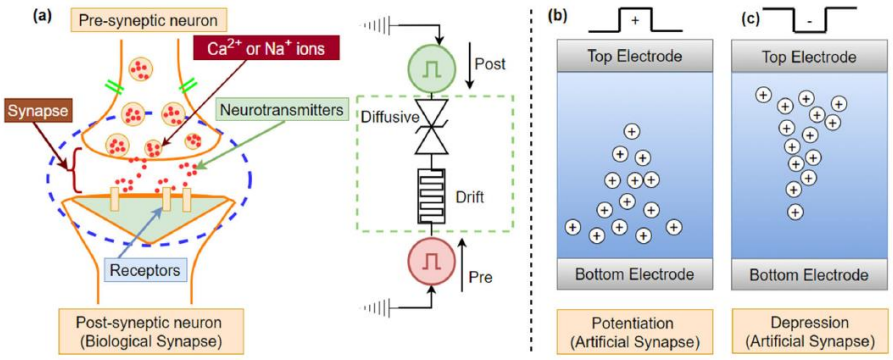

Figure 2. Presents a comparative analysis of biological and artificial synaptic systems(Gökgöz, Aydın, et al., 2024).

Inspired by the structural and operational principles of the human brain, neuromorphic computing aims to emulate hierarchical neural networks directly within hardware architectures. This paradigm involves mimicking the synaptic connections, temporal dynamics, and adaptive learning processes of biological neurons, while integrating machine learning algorithms into the physical design of the computational system (Schuman et al., 2017). Numerous neuromorphic processors have been developed using standard CMOS (Complementary Metal-Oxide-Semiconductor) technology, employing digital or mixed-signal circuits to simulate neuronal activity. Such artificial neural processing units enable the implementation of hardware-based neural networks, presenting a viable framework for systems capable of real-time adaptive learning.

To ensure scalable efficiency and enhanced learning performance in CMOS-based neural architectures, integrated memristive components must facilitate on-chip learning, particularly for supervised training paradigms (Gökgöz, Aydın, et al., 2024; Sung et al., 2018). Memristors, owing to their non-volatile storage properties and analog programmability, are considered pivotal for embedding biologically plausible learning mechanisms directly into hardware. Their unique attributes help narrow the divide between traditional digital circuitry and adaptive neuromorphic computing systems, enabling more brain-like functionality at the device level.

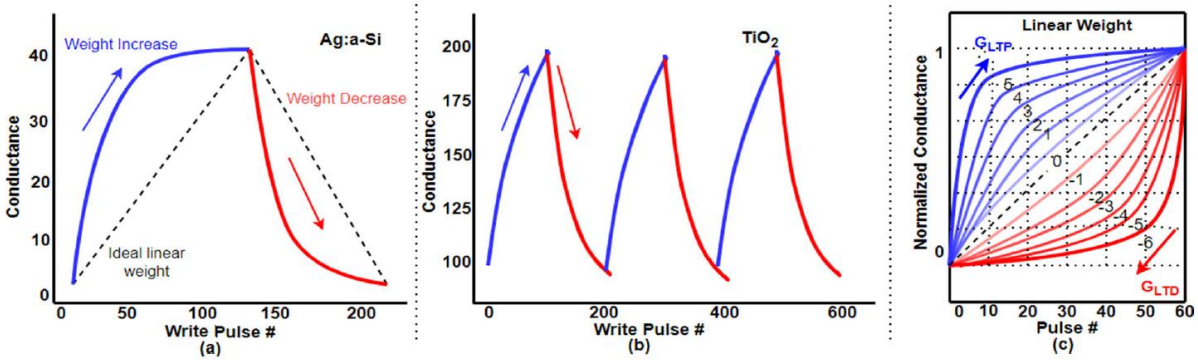

Figure 3. (a) Nonlinear weight update characteristics in Ag:a-Si-based devices, (b) Nonlinear weight modulation observed in TiO_2 memristive systems, (c) Behavioral model schematic of an analog embedded non-volatile memory (eNVM) device, illustrating nonlinear weight updates across a defined range (−6 to 6).

According to theoretical models, synaptic weight adjustments should scale linearly with the number of programming pulses, where each successive pulse induces a predictable, proportional conductance change. However, experimental observations reveal significant deviations from this ideal behavior in physical memristive and neuromorphic devices. Notably, the initial phases of synaptic plasticity mechanisms – including Long-Term Potentiation (LTP) and Long-Term Depression (LTD) typically demonstrate abrupt conductance variations. This nonlinear response progressively attenuates with

continued stimulation, ultimately reaching a saturation regime where additional pulses yield diminishing returns in weight modification.

In principle, synaptic weight updates should exhibit a linear dependence on the number of applied write pulses; however, experimental devices often demonstrate nonlinear behavior. Specifically, conductivity undergoes rapid modulation in the early phases of long-term potentiation (LTP) and long-term depression (LTD), eventually approaching saturation at higher pulse counts. As depicted in Fig. 3(a), (b), and (c), these nonlinearities introduce deviations that can compromise the precision and operational efficacy of neuromorphic computing systems.

III. IMPLEMENTATION OF ARTIFICIAL SYNAPSES IN NEUROMORPHIC COMPUTING ARCHITECTURES

In biological neural systems, synaptic connections serve as critical pathways for inter-neuronal communication, facilitating adaptive learning through plasticity mechanisms like long-term potentiation (LTP) and depression (LTD). Drawing inspiration from these natural processes, memristive artificial synapses are engineered to replicate such adaptive behavior by modulating their conductive states in response to spatiotemporal electrical stimuli. This tunable resistance characteristic effectively mirrors the experience-dependent plasticity inherent to biological synapses.

Resistive State Modulation: The synaptic weight update mechanism in memristive devices is characterized by a state-dependent transformation function, where conductance variations emerge from the dynamic interplay between the device's inherent memory state and externally applied electrical excitation:

$$R(t) = R_0 + \Delta R.f(W(t)) \quad (1)$$

here, R_0 denotes the initial or baseline resistance, ΔR indicates the maximum achievable variation in resistance, and $f(W(t))$ represents a state-dependent function governing the dynamic resistance modulation (see Eq. 1). This dynamic programmability allows memristive synaptic devices to adjust their conductance states based on historical electrical stimulation patterns, thereby emulating the activity-dependent plasticity observed in biological synapses (Wan et al., 2019). In neural network implementations, memristive synapses serve as programmable replacements for traditional passive components, offering distinct advantages due to their nonvolatile memory characteristics. Crucially, their inherent capability to undergo analog resistance modulation facilitates the hardware realization of neurobiological learning rules, including spike-timing-dependent plasticity (STDP) a Hebbian learning paradigm where coactive pre- and postsynaptic neuronal firing strengthens synaptic efficacy. Such biomimetic functionality renders memristive synapses particularly suitable for neuromorphic computing applications that demand embedded learning capabilities and adaptive synaptic reconfiguration (Malhotra & Singh, 2023).

To effectively model the nonlinear dynamics of synaptic plasticity, researchers have developed specialized behavioral modeling approaches. Among these, the MLP + NeuroSim co-simulation platform has emerged as a prominent tool for investigating real-time learning processes in neuromorphic architectures (Chen et al., 2018). This integrated simulation environment provides comprehensive analysis of neuromorphic hardware implementations incorporating analog emerging memory technologies, including but not limited to TiO_2 memristive synapses. The platform facilitates quantitative evaluation of key performance metrics such as power dissipation, computational latency, and layout area requirements. The underlying mathematical formulation captures the progressive modification of synaptic conductance (G) as a function of applied programming stimuli (P) through the following system of equations:

$$G_{LTP} = B\left(1 - e^{\left(-\frac{P}{A}\right)}\right) + G_{min} \quad (2)$$

$$G_{LTD} = -B\left(1 - e^{\left(-\frac{P-Pmax}{A}\right)}\right) + G_{max} \quad (3)$$

$$B = (G_{max} - G_{min})/(1 - e^{-P_{max/A}}) \quad (4)$$

Equations (2) and (3) define the conductance values corresponding to Long-Term Potentiation (LTP) and Long-Term Depression (LTD), denoted as G_{LTP} and G_{LTD}, respectively. The parameters G_{max}, G_{min}, and P_{max} are extracted from empirical measurements and represent the upper and lower bounds of the conductance range, as well as the maximum number of programming pulses required to transition between these two states. The parameter A determines the degree of nonlinearity in the weight update profile, where its sign indicates the direction of change positive for LTP (typically shown in blue) and negative for LTD (typically shown in red). Although the absolute value of A remains the same for both potentiation and depression, the polarity distinguishes the respective update directions. The parameter B, which is mathematically derived from A, serves to constrain the conductance modulation within the experimental limits defined by G_{max}, G_{min}, and P_{max}, as shown in Equation (4).

Biological neural networks exhibit a compartmentalized organization, where each structural component finds direct correspondence in artificial neural implementations and synaptic device designs. In this bioinspired paradigm, dendritic arbors operate as specialized input modules, transducing electrochemical signals from presynaptic neurons. The somal compartment performs spatial-temporal integration of these afferent signals, executing threshold-based firing decisions. Upon activation, the resulting action potential propagates through axonal projections, which function as conductive transmission lines. These terminate at synaptic clefts specialized neurochemical interfaces that facilitate signal transduction to subsequent dendritic receivers, thereby establishing complex, reconfigurable neural pathways (Sarker, 2021).

IV. COMPARATIVE ANALYSIS

The efficacy of artificial synaptic devices can be evaluated through the Modified National Institute of Standards and Technology (MNIST) database, an established benchmark in handwritten digit classification. While frequently associated with LeCun et al.'s seminal work, the dataset's conceptual foundations derive from R.A. Fisher's pioneering statistical pattern recognition research in the 1930s. The corpus comprises 10-class grayscale numeral representations (0-9), with original specimens captured at 48 × 48 pixel resolution (Sarker, 2021). To accommodate neuromorphic hardware constraints and computational efficiency, each image undergoes standardized preprocessing including digitization and spatial reduction to 28 × 28 pixels ensuring compatibility with neuromorphic system input specifications.

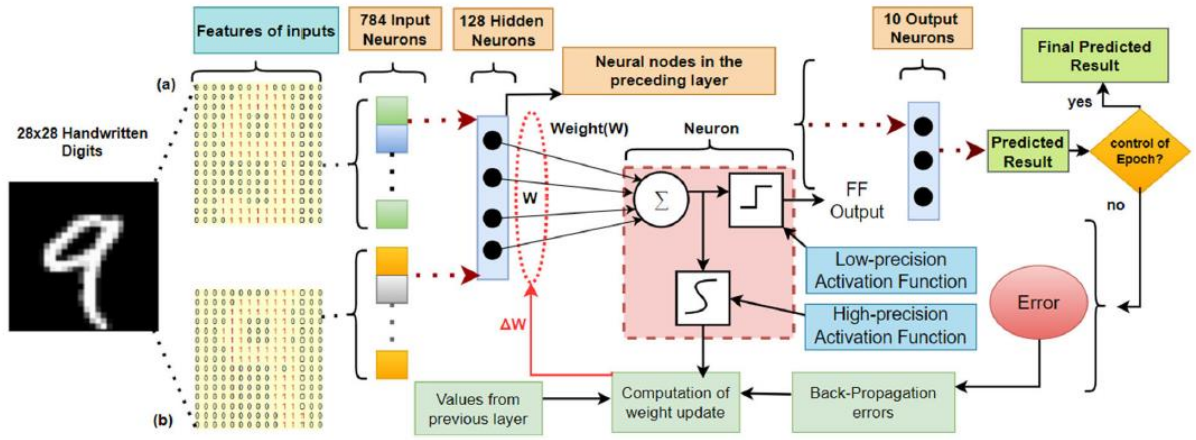

Figure 4. Multilayer Perceptron (MLP) Neural Network: The architecture of the implemented backpropagation neural network (BPNN) and its constituent neurons are illustrated. (a) A 28×28 binary matrix depicting a computer-simulated digit, and (b) a corresponding handwritten digit sample.(Gökgöz, Aydın, et al., 2024)

For comparative performance analysis, a minimal two-layer multilayer perceptron (MLP) architecture was implemented as a reference model. The network topology, depicted in Figure 4, features three fundamental structural elements: (1) an input layer for data ingestion, (2) a hidden layer for feature

transformation, and (3) an output layer for classification decisions. Employing full inter-layer connectivity (dense architecture), each computational unit establishes synaptic connections with all neurons in the subsequent layer, thereby enabling the extraction of hierarchical feature representations. These trainable connection weights, which modulate inter-neuronal signal propagation, provide the mathematical foundation for the network's adaptive learning capacity and representational flexibility.

To improve the operational efficiency of the designed TiO_2-based synaptic device, various optimization techniques were applied. The performance evaluation was carried out using a combination of custom-developed software and the NeuroSim simulation framework [26], which enabled accurate modeling of device behavior under neuromorphic workloads. The implementation of the neural network model was tested on a computing system equipped with an Intel Core i7-10750H processor (2.60 GHz) and 8 GB of RAM to assess energy consumption and classification accuracy.

Although the TiO_2 synapse-based neural network demonstrates longer training latency compared to conventional software-based convolutional neural networks (CNNs), it significantly outperforms them in terms of energy efficiency. When trained using the Adam optimization algorithm, the memristive model achieved a competitive classification accuracy of approximately 92%. While this is marginally lower than the 96% accuracy achieved by its traditional CNN counterpart, the dramatic reduction in energy consumption positions the TiO_2-based model as a compelling solution for power-constrained environments.

As illustrated in Table I, the conventional CPU-based neural network consumes nearly 100,000 times more energy than the memristive synaptic device-based implementation, underscoring the substantial benefits of memristor technology in energy-sensitive AI applications.

Table 1. Benchmarking Energy and Accuracy: Memristive Synaptic Devices Versus Traditional Processors

Device Type	**Performance Metrics**	
	Accuracy	***Energy Consumption***
Artificial Synaptic Hardware	92%	0.04421(J)
Traditional Computer	96%	4.275*103(J)

V. CONCLUSION

In conclusion, the integration of memristive synapses into neuromorphic computing architectures emerges as a compelling and forward-looking strategy for mitigating the substantial energy inefficiencies associated with traditional Von Neumann computing systems. Memristive devices, characterized by their intrinsic capability to emulate the dynamic and plastic nature of biological synapses, provide a promising foundation for constructing next-generation computing platforms that prioritize both energy efficiency and scalability. These devices operate with minimal power consumption and offer non-volatile, analog memory features that are highly conducive to in-memory computation, thereby alleviating the performance bottlenecks caused by the separation of memory and processing units in conventional architectures. As the limitations of CMOS scaling, thermal management, and interconnect delays continue to hinder the performance gains of conventional multicore and semiconductor-based technologies, memristor-enabled neuromorphic systems present a transformative alternative. Their biologically inspired design principles not only facilitate real-time learning and parallel information processing but also hold significant potential to accelerate the development of more intelligent, autonomous, and energy-conscious artificial intelligence hardware solutions.

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