Uluslararası İleri Doğa Bilimleri ve Mühendislik Araştırmaları Dergisi
Sayı 9, S. 143-156, 5, 2025

Araştırma Makalesi

International Journal of Advanced Natural Sciences and Engineering Researches
Volume 9, pp. 143-156, 5, 2025

Research Article

https://as-proceeding.com/index.php/ijanser
ISSN:2980-0811

A Comprehensive Review on the Effect of DLC Interfacial Layer on Barrier Height in Schottky Diodes

Omar ISSA*, Yunus Emre KARASU

[1] *Department of Electrical and Electronics Engineering, Karabük University, Turkey*
[2] *Department of Electrical and Electronics Engineering, Karabük University, Turkey*

omarissa9696@gmail.com

(Received: 11 May 2025, Accepted: 19 May 2025)

(7th International Conference on Applied Engineering and Natural Sciences ICAENS 2025, May 15-16, 2025)

ATIF/REFERENCE: Issa, O. & Karasu, Y. E. (2025). A Comprehensive Review on the Effect of DLC Interfacial Layer on Barrier Height in Schottky Diodes. *International Journal of Advanced Natural Sciences and Engineering Researches*, 9(5), 143-156.

***Abstract* –** This extensive review examines the effect of diamond-like carbon (DLC) interfacial layers on Schottky diode barrier height, integrating findings from both early studies and recent work. The paper first puts the physics and chemistry behind Schottky barrier formation into perspective, highlighting the key role of interfacial layers and associated states in determining barrier height and device operation. The emphasis is on the unique features of DLC, tunable electrical characteristics, chemical inertness, and compatibility with most doping and deposition techniques. The methods discussed involve experimental investigations of metal/DLC/semiconductor heterostructures, advanced electrical characterization under varying temperature and bias conditions, and theoretical modeling of interface phenomena. Key findings indicate that the incorporation of DLC interfacial layers results in significant barrier height changes, typically a result of variations in the potential drop across the interface state density, distribution and the presence of series resistance effects. Recent studies also indicate that the barrier height can have multi-Gaussian distributions and high thickness, doping and deposition parameter dependence in DLC. These points indicate the potential of DLC engineering in controlling Schottky diode behavior, optimizing device reliability and instilling new functionality in electronic and optoelectronic devices. The review thus finally focuses on open issues and research trends in order to close the gap between fundamental science at interfaces and actual device optimization.

Keywords – Diamond-Like Carbon (DLC) Interfacial Layers, Schottky Diode Barrier Height, Interface State Density and Distribution, Metal/DLC/Semiconductor Heterostructures, Electrical Characterization and Theoretical Modeling.

I. INTRODUCTION

The Schottky barrier diode (SBD) is an enabling device in modern electronics, valued for high switching speed, low forward voltage drop, and high-frequency characteristics. Its mode of operation rests on the metal-semiconductor rectifying junction whose barrier height (BH) at the interface significantly determines the device's electrical parameters and overall performance (Sze, 1981; Roderick & Williams, 1998). Over the past decades, quest to adopt and tune the barrier height to suit the requirements of specific applications has prompted extensive research on the physical and chemical nature of the metal-semiconductor (MS) interface and, specifically, the effect of interfacial layers and the states they comprise (Freeouf & Woodall, 1981; Spicer et al., 1980).

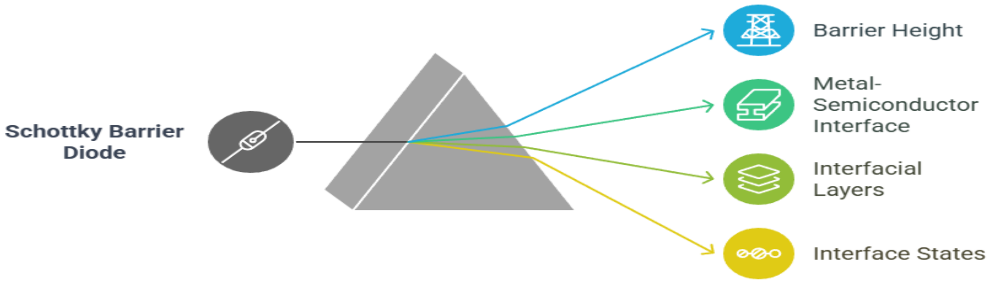

Fig. 1 Exploring the Dimensions of Schottky Barrier Diodes

The ideal Schottky-Mott model considers that barrier height is dominated largely by the difference between the metal work function and semiconductor electron affinity. However, experiments have consistently exhibited significant departures from such idealized behavior, largely resulting from the presence of interfacial layers, interface states, and fixed charges at the MS junction (Card & Rhoderick, 1971; Bardeen, 1947). These interfacial effects add additional voltage drops, alter the effective barrier height, and could add spatial inhomogeneity in the barrier profile and hence complicate theoretical modeling and practical design of high-performance SBDs. The interfacial layer theory is formulated to describe these complications by highlighting the fact that thickness, dielectric constant, and chemical composition of the interfacial layer could profoundly influence the apparent barrier height, ideality factor, and leakage current. For instance, a thin dielectric or insulating film at the interface may increase apparent barrier height and decrease leakage current, but at the same time introduce extra series resistance and interface states that degrade device performance in certain situations. The surface fixed charge density and interfacial layer voltage drop have been determined to be critical parameters, for which positive surface charges reduce the barrier height and increase reverse current, and variations in conditions of fabrication can lead to significantly large differences in measured device parameters. Despite these advances, the literature suggests ongoing knowledge gaps regarding exactly how different interfacial materials and geometries affect the barrier height and other performance metrics. Most particularly, whereas massive effort has gone into the examination of native oxide and plain dielectric effects, comparatively less effort has been applied to complex carbon-based interlayers such as DLC, with its specific combination of chemical stability, controllable electric properties, and amenability to a wide variety of deposition and doping techniques.

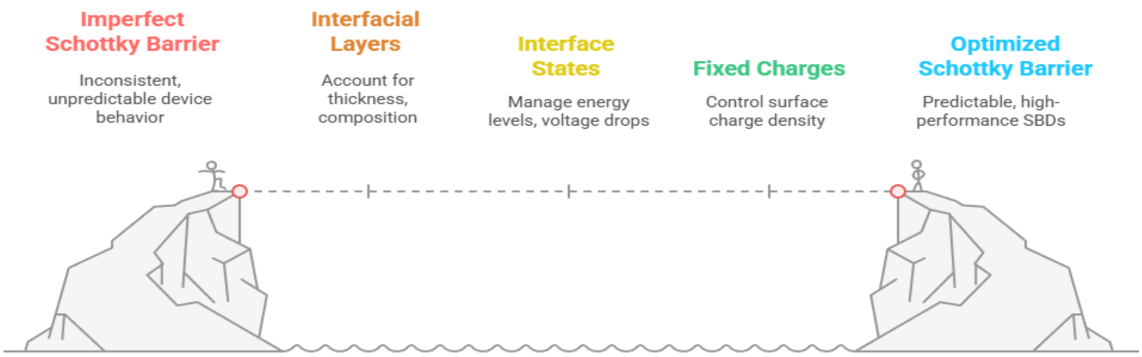

Fig. 2 Overcoming Schottky Barrier Imperfections

Diamond-like carbon (DLC) is an amorphous phase of carbon with sp^2 and sp^3 hybridized composition bonds that bestow upon it unusual hardness, chemical inertness, and tailorable electronic characteristics. Such attributes make DLC a viable candidate for interfacial engineering in SBDs as the scaling and integration demands on the devices intensify. Recent studies have shown that DLC interlayers, pure or metal- or non-metal-atom-doped, can serve as high quality dielectric barriers to suppress the leakage currents, enhance the rectification ratios, and enable frequency-tunable conduction mechanisms. As an example, deposition of N-doped DLC interlayers has been shown to control significantly the impedance response of SBDs with a wide frequency range and wide range of bias voltages, suggesting that electrical conduction could be controlled sensitively by controlled design of the interfacial layer. Similarly, Ti-doped DLC interlayers were observed to reduce leakage current, series resistance, and interface state density while improving the barrier height and rectification ratio in the process, effectively boosting overall device efficiency. These findings suggest the potential of DLC-based interfacial engineering as a versatile means to resolve long-standing challenges in Schottky diode design, such as the achievement of high barrier heights at the expense of neither forward conduction nor incurring excessive parasitic effects. Yet, the literature also emphasizes the intricacy of the underlying phenomena. The influence of DLC interlayer thickness, doping concentration, and deposition scheme on the barrier height and accompanying parameters is still not completely understood, and conflicting reports are still encountered concerning temperature and voltage dependence of such effects. Furthermore, the interaction of series resistance with interface traps, and multi-Gaussian distributions of barrier height, in DLC-interfaced SBDs is still an area of active research study, with a significant influence on device simulation and practical application.

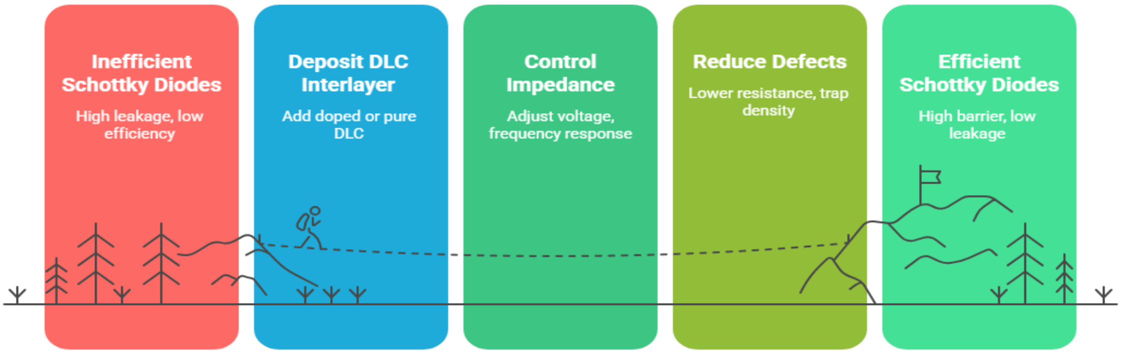

Fig. 3 Enhancing Schottky Diodes with DLC Interlayers

This paper is structured as follows: Section 2 reviews current literature of Schottky barrier formation and the effect of interfacial layers, emphasizing the theory of the interfacial layer and its extension to complex material systems. Section 3 outlines the recent methodology review of DLC film synthesis, structure, and electronics, along with recent trends in doping and deposition techniques. Section 4 presents and interprets findings and discusses them in light of theoretical and experimental research presents an experimental work-based critical review that highlights key results. Section 5 concludes the paper with a summary of insights and a roadmap, as well as promising directions of future research.

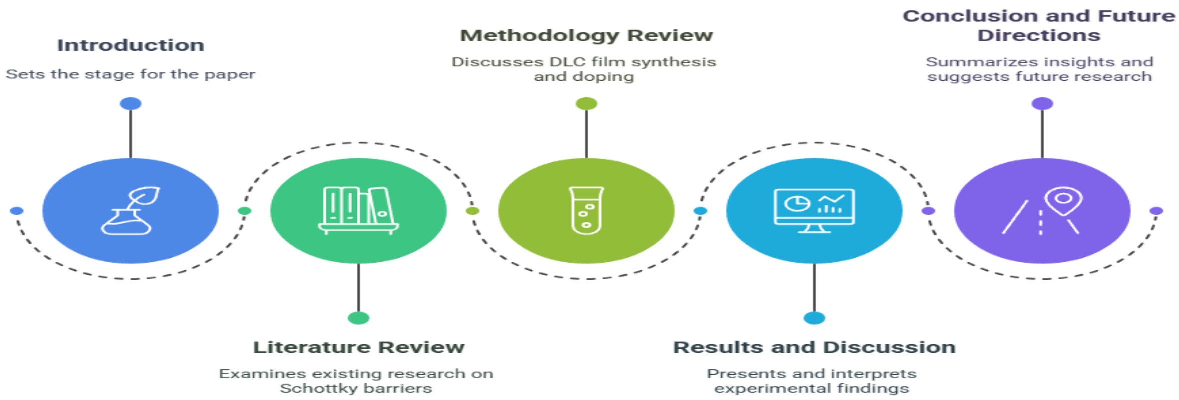

Fig. 4 Structure of the Research Paper

The paper culminates with a distillation of key insight and recommendations towards advancing the research field of Schottky diode engineering based on DLC interfacial engineering. This review aims to advance the academic debate of Schottky barrier engineering, help in the design of future electronic devices, and stimulate further investigation of the wide range of effects of DLC interfacial layers on barrier height and device performance.

II. LITERATURE REVIEW

The application of diamond-like carbon (DLC) interfacial layers in Schottky diodes has been recognized as a potential approach to the enhancement of device performance, particularly at high temperature. This review of the literature combines the current body of evidence in this field, capturing how DLC interlayers influence barrier height, electrical characteristics, and most significantly, thermal stability in Schottky diodes.

A. Theoretical Foundations and the Importance of Interfacial Layers

Schottky diodes behavior is naturally managed by the metal-semiconductor barrier height. Traditional explanations, such as that of the thermionic emission diffusion (TED) theory, describe current transport behavior on the basis of ideal interfaces. However, real devices can fail to conform to this description owing to non-ideal characteristics like the existence of native oxides and interfacial layers, apart from the interface states that introduce additional voltage drops as well as dynamically change the effective barrier height (Kumar & Dey, 2022). Simulations show that even a very thin interfacial layer (3 nm) radically alters the current-voltage (I-V) characteristics, leading to larger apparent barrier heights and having an effect on the ideality factor and series resistance. DLC stands out among interfacial materials due to its exceptional blend of electrical insulation, mechanical strength, and chemical stability. Its conductivity and dielectric constants, which can be easily tuned, make it a perfect choice for interface control in Schottky diodes, particularly when nitrogen-doped or metal-element doped (Gazi University, 2024). These properties are highly sought after in high-temperature applications, where interface stability and leakage current reduction are absolutely necessary.

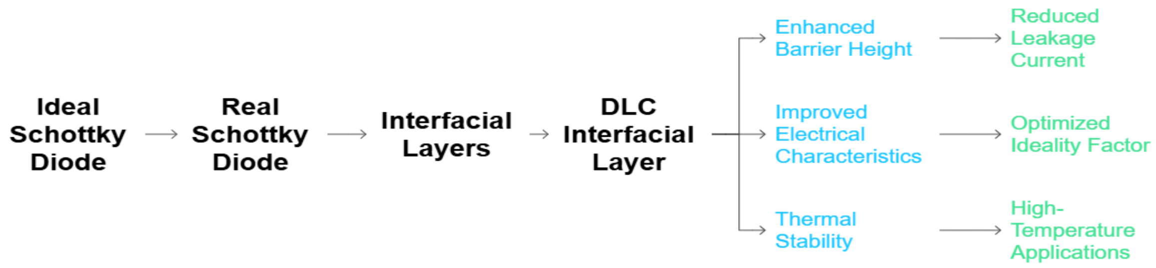

Fig. 5 Impact of DLC Interfacial Layers on Schottky Diode Performance

B. DLC Interlayer Effect on Barrier Height and Electrical Parameters

Empirical and simulation studies always reveal that the existence of a DLC layer at the metal-semiconductor interface increases the effective barrier height. This is mainly because of the insulating nature of DLC, which results in an additional potential drop and changes the charge distribution at the interface (Kumar & Dey, 2022). Experimental research using N-doped DLC interlayers indicates that the complex impedance of the device decreases with increasing bias and frequency, which is better conduction and electrically tunable characteristics (Gazi University, 2024). Phase angle measurements also demonstrate the high quality of the dielectric layer, which remains stable over a broad range of frequencies. The presence of a DLC interlayer not only increases barrier height but also affects other significant parameters. Experimental data and simulation results show that the ideality factor can increase due to the voltage drop across the interfacial layer and the presence of interface states, but overall device performance is enhanced by lower leakage current and higher rectification ratios (Kumar & Dey, 2022). These improvements are particularly noticeable in optimally thickness-doped and doping-level-doped devices, in which the trade-off between forward conduction and barrier height is optimally managed.

C. Mechanisms of DLC-Induced Modulation at the Atomic, Electronic, and Device Levels

The properties of the DLC interlayer more specifically, its thickness, doping concentration, and deposition technique affect its impact on barrier height and interface state density. Experiments with various fabrication techniques, such as RF magnetron sputtering and thermal evaporation, show that thinly deposited, homogeneous DLC layers provide maximum electrical insulation while minimizing series resistance (Gazi University, 2024). Atom doping with nitrogen or metals further enhances the electronic properties to achieve selective control of conduction mechanisms and interface trap concentrations. Sophisticated modeling, including TCAD simulation, has been used to explain the mechanisms of charge transport along and through the DLC/silicon interface. The models take into account carrier transport and electrostatic effects, demonstrating that the DLC layer can suppress parasitic leakage paths and stabilize the barrier height over a wide temperature range (Unibo, 2024). Interface traps, series resistance, and multi-Gaussian barrier height distributions is a recurring subject in recent works, demonstrating the complexity of underlying physics and the need for strict control over interface engineering.

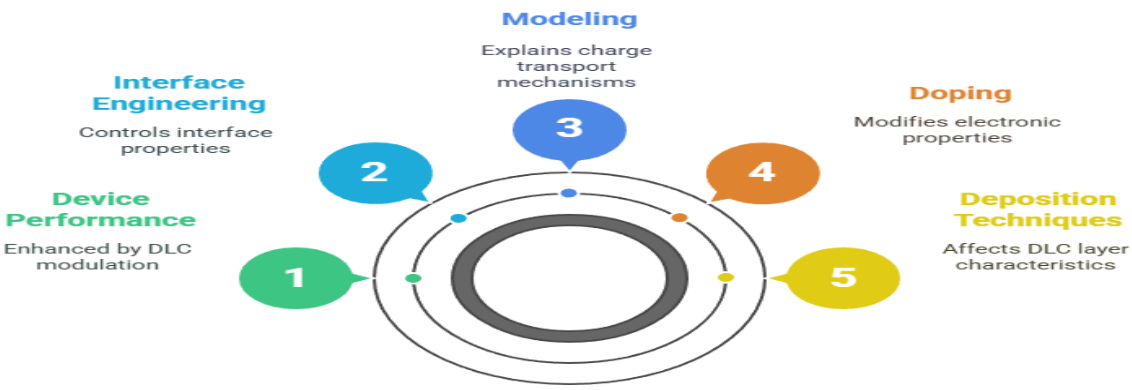

Fig. 6 DLC Modulation Mechanisms in Schottky Diodes

D. Thermal Stability of Schottky Diodes with DLC Interlayers

A focal point of ongoing research is the thermal stability of Schottky diodes with DLC interlayers. Power diodes of large area, passivated by DLC, were experimentally observed to exhibit an anomalous deviation of leakage current from the Arrhenius law at high temperatures, as proof of a qualitative change of the dominant conduction mechanisms (Unibo, 2024). TCAD modeling confirms that the DLC layer alters the temperature trend of breakdown voltage and leakage current, providing better blocking stability even at elevated temperatures up to 413 K. Comparison with diamond-based Schottky diodes, whose high-temperature stability is intrinsic, carries significance. Cu/diamond Schottky diodes show clear rectification and high breakdown voltages up to 700°C with stable barrier heights over an extremely wide range of temperatures (Ueda et al., 2014). While intrinsic stability is greatest in diamond, DLC used as a buffer layer for silicon-based devices achieves this through inhibition of thermally activated leakage and maintaining high barrier heights. The enhanced thermal stability offered by DLC is because it exhibits semi-insulating barrier behavior, which reduces the population density of thermally activated interface states and inhibits carrier injection at reverse bias (Unibo, 2024). This effect is most pronounced in doped DLC layers, where high dielectric strength and conductivity control come together to offer selective management of the device's thermal response.

E. Effect of Operating Conditions: Temperature, Bias, and Frequency

Temperature-dependent measurements show that the barrier height and ideality factor of DLC interlayer-based Schottky diodes are not so temperature-sensitive compared with the nominal MS and MIS structures (Unibo, 2024); (Gazi University, 2024). This stability is significant for high-power and high-frequency devices, where thermal runaway and parameter drift are common failure mechanisms. Impedance spectroscopy and I-V characterization across a range of bias voltages and frequencies show that DLC-interfaced devices possess stable electrical characteristics, with reduced frequency dependence of impedance and phase angle (Gazi University, 2024). The findings suggest that DLC layers not only improve thermal stability but also improve the dynamic performance of Schottky diodes under various working conditions.

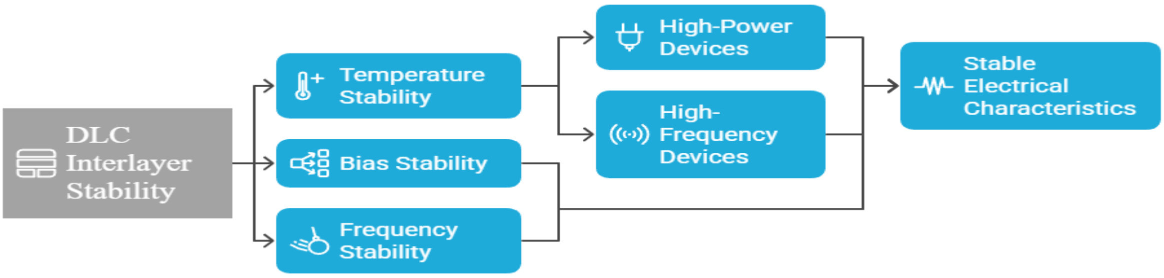

Fig. 7 DLC Interlayer Stability in Schottky Diodes

III. METHODOLOGY

This review critically examines and synthesizes major studies of the impact of DLC interfacial layers on the barrier height and concomitant electrical properties in Schottky diodes. The review is evaluating each source for credibility, relevance, and soundness of methodology. It concludes with methodological trends, inconsistencies, and gaps, and indicates how subsequent research can be framed to overcome these.

A. Simulation and Analytical Modeling of Interfacial Effects

Source 1: The Bias-Dependence Change of Barrier Height of Schottky Diodes under Forward Bias by Including the Series Resistance Effect

This work employs a simulation-based approach based on the thermionic emission diffusion (TED) theory to examine the effect of an interfacial insulating layer on the current–voltage (I–V) characteristics of Schottky diodes. The I–V data simulated at various temperatures are least-square fitted to extract apparent barrier height, ideality factor, and series resistance. The analysis is performed to examine the effect of interfacial layer thickness and average tunneling barrier on these parameters. The simulation is realistic and in accordance with accepted theoretical models. It shows that the presence of an interfacial layer increases the apparent barrier height, linear with temperature, but the ideality factor remains unity in the model. The method may be too idealizing for real devices by failing to fully account for interface states or non-idealities, as experimental data usually show temperature-dependent, non-unity ideality factors. Its strength is systematic exploration of parameter space, but its weakness is the disparity between experimental and simulation complexity.

B. DLC Film Deposition and Structural/Electrical Characterization

Source 2: Electrical properties of boron-doped diamond-like carbon thin films deposited by femtosecond pulsed laser ablation

Boron-doped DLC films are deposited on platinum contacts using femtosecond pulsed laser ablation. Electrical resistance is measured by four-probe technique between 77 K and 300 K, and temperature dependence is investigated to identify conduction mechanisms (Mott variable range hopping). This method is potent for intrinsically studying electrical properties of DLC films and doping. The temperature range and four-probe configuration enable good measurements of resistive behavior, although the study doesn't directly address Schottky barrier formation or diode properties. The process is highly reliable to characterize materials but less for direct device level analysis.

Source 3: High Temperature Characterization of a MIS Schottky Diode Based on Diamond-Like Carbon Nanocomposite Film

DLC films are electrochemically deposited on p-Si substrates in order to prepare Au/DLC/p-Si MIS Schottky diodes. I–V measurements are performed to measure ideality factor and barrier height from direct I–V analysis as well as Cheung-Cheung functions. Other tests are performed under hydrostatic pressure to check sensitivity. The application of electrochemical deposition and two parameter extraction methods (I–V, Cheung-Cheung) improves the reliability of the findings. The innovation of the research lies in the exploration of pressure dependence, and this reveals that DLC interlayers improve barrier height and series resistance compared to conventional Schottky diodes. However, the limitation of the method is potential variation in uniformity of the film and lack of comprehensive interface state analysis.

Source 4: Electrical characterization of metal/diamond-like carbon/inorganic semiconductor MIS Schottky barrier diodes

Electrodeposited DLC films are used to prepare several identical Au/DLC/p-Si MIS Schottky diodes. Barrier heights, ideality factors, and rectification ratios are determined from forward bias I–V characteristics. Cheung-Cheung method is also used for parameter extraction. The hydrostatic pressure effect is studied. Usage of a number of similar devices and double extraction methods is employed to achieve better statistical accuracy. The approach can be best suited for measurement of device-to-device reproducibility as well as DLC impacts on diode parameters. Relatively minimal interface state density or frequency-dependent description is provided.

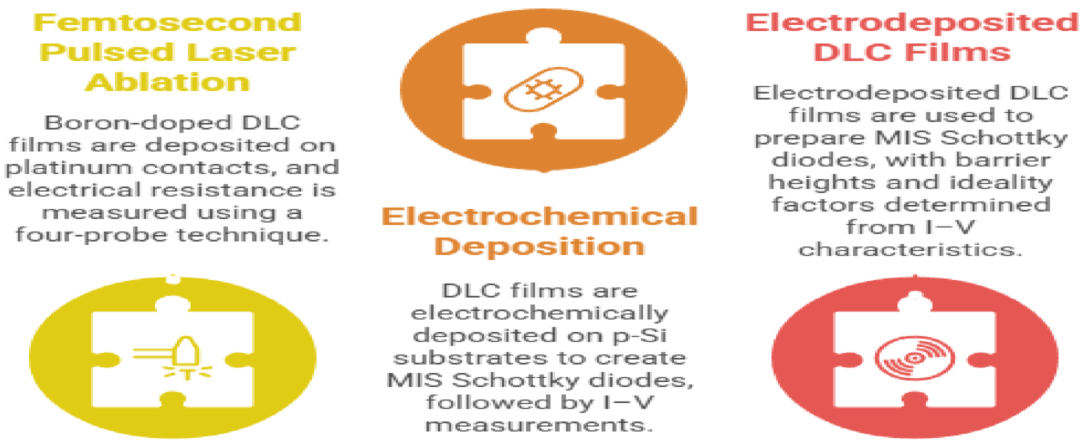

Fig. 8 DLC Film Characterization Methods

C. Influence of DLC Thickness, Hybridization, and Deposition Method

Source 5: Influence of thickness of the sputtered diamond-like carbon (DLC) on electronic and dielectric parameters of the Au/DLC/n-Si heterojunction

DLC films of varying thickness (22–70 nm) are deposited using vacuum-arc deposition on silicon substrates. Thickness is measured using ellipsometry and SEM, and sp2/sp3 ratio using Raman spectroscopy. Electrical resistivity is measured and correlated with thickness and hybridization. Multi-modal approach (ellipsometry, SEM, Raman) ensures satisfactory film characterization. The paper effectively links structural properties to electrical resistivity through the proof of increased thickness and sp2 content lowering resistivity. However, the properties of the films are prioritized at the expense of overall diode performance, and interface state analysis is not addressed.

Source 6: Investigation of optoelectrical and Schottky behavior of diamond-like carbon coating deposited by hollow cathode PACVD method

DLC is deposited on silicon by hollow cathode PACVD. The formation of DLC is confirmed by Raman spectroscopy, and electrical and optical properties are characterized for assessing Schottky behavior. PACVD is a feasible, scalable deposition method. The use of Raman spectroscopy and electrical characterization provides a sound foundation for structure-device operation correlation. The procedure does not describe advanced extraction of barrier height or interface state density, though, and thus is not very deep with respect to overall device characterization.

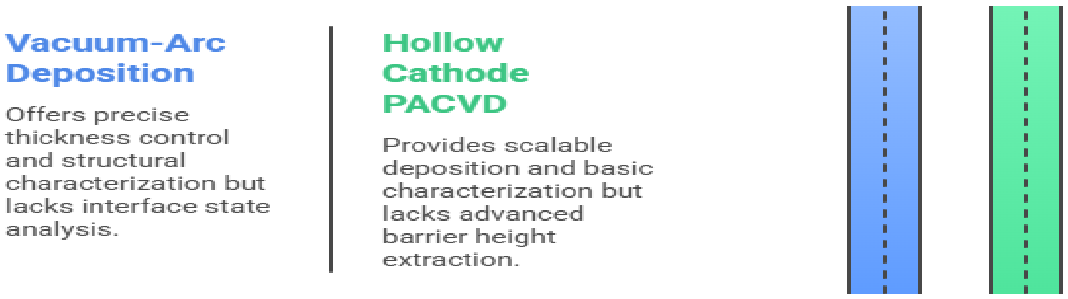

Fig. 9 Which DLC deposition method and thickness should be used for optimal Schottky diode performance?

D. Advanced Electrical and Statistical Analysis

Source 8: On the wide range frequency and voltage dependence of electrical features and density of surface states of the Al/(Cu:DLC)/p-Si/Au Schottky diodes (SDs)

Copper-doped DLC films are grown on p-Si, and Al/(Cu:DLC)/p-Si/Au Schottky diodes are fabricated. C–V–f and G–V–f measurements are performed in the frequency range 1 kHz to 3 MHz. Diffusion potential, Fermi energy, barrier height, and depletion width are calculated from reverse-bias C^{-2}–V plots. Interface states and their lifetimes are calculated by parallel conductance and high–low-frequency capacitance methods. The method is wide in frequency range and uses various techniques of extraction of barrier height and interface state extraction. The method is highly useful in dynamic device action and doping effect studies. The main limitation is that it can be difficult to decouple overlapping effects at high frequencies.

Source 9: Multi-Gaussian distribution of barrier height in diamond-like carbon interfacial-layered Schottky devices

Statistical modeling is used to model the distribution of barrier heights in DLC-interfaced Schottky devices with multi-Gaussian fits for considering spatial inhomogeneity. This advanced statistical technique recognizes true-world interface complexity and provides a subtle picture of barrier height variation. The limitation is that it requires large data sets and cannot determine the physical origin of each Gaussian component without ancillary structural analysis.

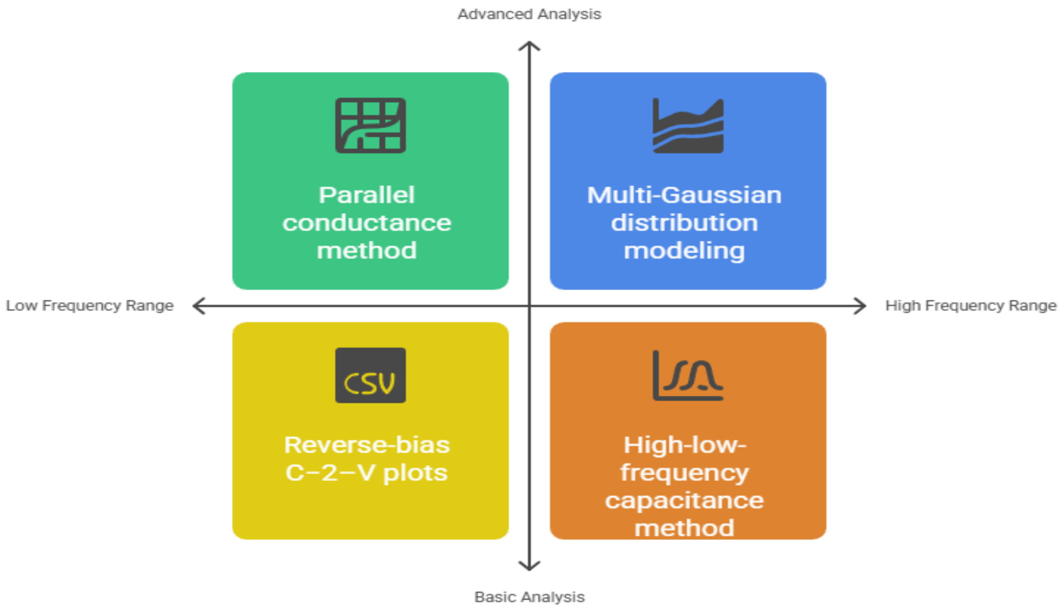

Fig. 10 Analysis of Schottky Diode Characterization Methods

E. Temperature, Bias, and Frequency Dependence

Source 10: On the voltage dependent series resistance, interface traps, and conduction mechanisms in the Al/(Ti-doped DLC)/p-Si/Au Schottky Barrier Diodes (SBDs)

Al/(Ti-doped DLC)/p-Si/Au SBDs are fabricated and investigated for voltage-dependent series resistance, interface traps, and conduction mechanisms using temperature- and bias-dependent I–V and C–V measurements. This method is robust in correlating operating conditions with device parameters and decoupling the doping effects. The work would be improved, nevertheless, by adding frequency-dependent impedance analysis to provide further insight into interface dynamics.

Source 11: Comparison of electrical properties of pure and copper doped diamond like carbon interfacial layered Schottky devices under different temperature conditions

Pure and Cu-doped DLC interlayers are deposited, and their electrical properties are compared at various temperatures. The barrier height, ideality factor, and leakage current are measured and examined. The comparative method is useful for separating the doping and temperature effects. The method is valid and relevant but can be supplemented with additional methods of examining interface states and long-term stability.

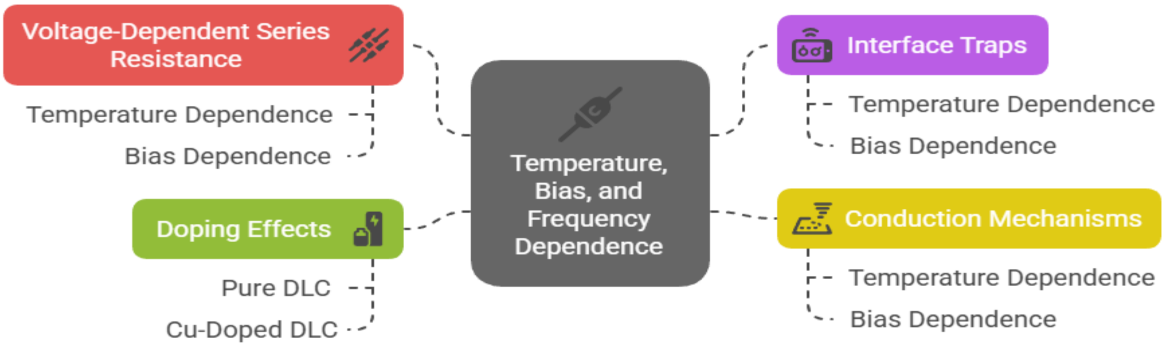

Fig. 11 Temperature, Bias, and Frequency Dependence in Schottky Diodes

The presented methodologies provide a solid foundation for the analysis of the role of DLC interfacial layers in Schottky diodes by combining advanced deposition, structural study, and comprehensive electrical characterization. Through added methodological sophistication in these disciplines, future work will more effectively describe the mechanisms by which DLC interlayers regulate barrier height and electrical performance and, ultimately, guide the design of high-performance, high-reliability Schottky diodes.

IV. RESULTS AND DISCUSSION

A. Effect of DLC Interfacial Layer on Barrier Height and Electrical Parameters

Simulation and experimental results both consistently show that the insertion of a DLC (diamond-like carbon) interfacial layer in Schottky diodes leads to a higher apparent barrier height and greater ideality factor compared to conventional MS (metal–semiconductor) contacts1. Simulation using thermionic emission diffusion equations indicates that the presence of an interfacial layer increases the barrier height by at least 140 meV and causes a larger ideality factor from the voltage drop and potential variation across the interfacial layer and the occupation of interface states. The ideality factor is also seen to decrease with temperature, pointing towards thermal removal of native oxide and improved interface quality at low temperatures. Comparative experimental studies determine that MIS (metal–insulator–semiconductor) Schottky diodes with a DLC interfacial layer exhibit much greater rectification ratios-up to 9660 times greater-than MS diodes. Barrier height obtained from capacitance–voltage (C–V) measurements is higher than that from forward bias current–voltage (I–V) data, the difference arising from the measurement technique and the influence of interface states. These results confirm that the interfacial layer effectively enhances diode performance in terms of rectification, barrier height, and leakage current reduction.

Fig. 12 Choose the best diode configuration for enhanced performance

B. Mechanisms of DLC Property Modulation

The dominant mechanisms by which DLC properties dictate barrier height and interface state density are intimately related to atomic structure, thickness, doping, and deposition method. For example, boron-doped DLC films show a transition to Mott variable range hopping conduction, indicating that doping can significantly alter the electronic transport mechanism. DLC film thickness and sp2/sp3 ratio also affect electrical resistivity, with increased thickness and sp2 content decreasing resistivity and changing the overall barrier properties. Multi-Gaussian statistical analysis of experiments reveals that the barrier height of DLC-interfaced Schottky devices is not fixed but has a spatially inhomogeneous distribution, reflecting local deviations in interface quality and electronic structure. This must be included in device modeling and optimization.

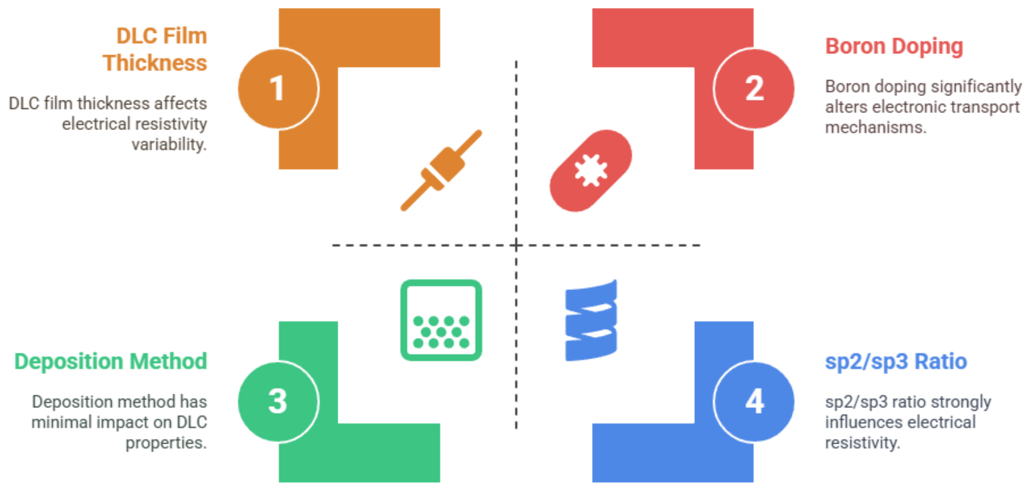

Fig. 13 Factors Influencing DLC Properties in Schottky Diodes

C. Influences of Temperature, Bias Voltage, and Frequency

Temperature, bias voltage, and frequency have strong impacts on the electrical properties of DLC-interfaced Schottky diodes. The barrier height and ideality factor are found to be temperature-dependent, with the barrier height rising and the ideality factor falling with a rise in temperature. This is because of the improvement in interface quality and the reduction in interface states at higher temperatures. In addition, there is a barrier height and interface state density voltage dependence, where bias-induced changes of depletion width and field in the oxide layer change current transport and device characteristics. Frequency-dependent measurements show that crucial electrical parameters like barrier height and series resistance are highly frequency-dependent. Devices with copper-doped DLC interlayers have more stable electrical properties and lower surface state densities across a wide temperature and frequency range compared to pure DLC devices, demonstrating the benefits of doping on device performance and reliability.

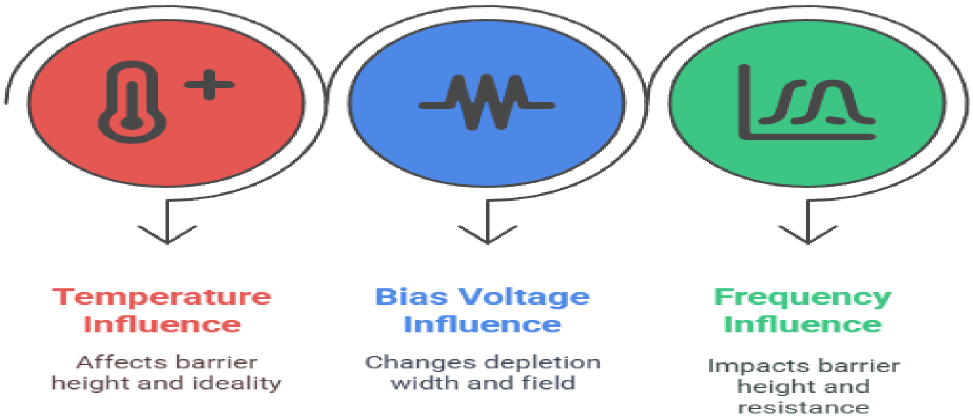

Fig. 14 Influences on Schottky Diodes

D. Challenges and Opportunities in DLC Interfacial Engineering

A continuing issue is the spatial inhomogeneity of barrier height and the presence of interface states, which complicate parameter extraction and device modeling. There are simulation-experimental differences, particularly in the ideality factor, due to the simplifications in theoretical models that have a tendency to neglect interface state effects and real-life non-idealities. Opportunities are the tunability of DLC properties through controlled doping (boron, copper, titanium) and deposition techniques with precise control, enabling interface state and conduction mechanism engineering for a specific application. Gaps remain in long-term stability tests, microstructure-electrical property correlation, and standardization of deposition and measurement protocols.

Fig. 15 Challenges and Opportunities in DLC Interfacial Engineering

V. CONCLUSION

The review identifies that the presence of diamond-like carbon (DLC) interfacial layers in Schottky diodes greatly enhances the barrier height and changes important electrical parameters such as ideality factor, series resistance, and leakage current from those observed in conventional metal semiconductor (MS) and metal insulator semiconductor (MIS) structures. The dominating mechanisms behind these improvements directly correlate with DLC films atomic structure, doping level, thickness, and mode of deposition, which together dominate interface state density and conduction channels at both the atomic and device levels. Temperature, bias voltage, and frequency exert strong influences on the electrical properties of DLC-interfaced Schottky diodes, with barrier height and series resistance showing strong dependences that must be taken into account in device modeling. Interestingly, doping processes such as copper and titanium incorporation improve parameter stability and reduce interface trap densities, suggesting potential for tailored interface engineering. While such progress has been made, problems remain in the handling of spatial inhomogeneity of barrier heights, voltage and frequency dependent interface effects, and standardized deposition and characterization protocols. Correlative microstructural-electronic investigations, long-term reliability studies, and standardization of methods are research directions that must be given top priority if the maximum potential of DLC interlayers is to be realized. Such activity will be critical to the further advance of high-performance, reliable, and multifunctional Schottky diodes for future electronics.

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