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Design and Simulation Analysis of a Novel Bidirectional 7-Level Multilevel Inverter Topology for Energy Storage Systems

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***Abstract*—**Conventional multilevel inverter (MLI) topologies, such as Neutral Point Clamped (NPC) and Cascaded H-Bridge (CHB), are widely utilized to improve power quality; however, they often require a high number of isolated DC sources and suffer from high switching losses and increased circuit complex- ity. To address these limitations, this paper presents a novel 7- level bidirectional MLI topology specifically designed for applica- tions requiring bidirectional power flow, such as energy storage systems (ESS) and mobile power storage units. The proposed topology utilizes a single DC source integrated with a capacitive voltage divider to generate the required intermediate levels. To minimize switching losses and computational complexity, a Modified Nearest Level Control (NLC) strategy is employed. The switching angles are analytically pre-calculated to synthesize a 7-level staircase waveform with minimized low-order harmonics, ensuring a fundamental output voltage that meets design speci- fications while inherently maintaining capacitor voltage balance through optimized state selection. This approach eliminates the need for high-frequency carriers, real-time reference tracking, or complex external balancing circuits. Performance of the topology was evaluated through extensive simulations at a 5 kW full-load operating point. The results demonstrate a remarkable efficiency of 98.8% in inverter and 98.5% in rectifier operating modes. By generating a 7-level staircase waveform at the output, the proposed configuration provides an effective power conversion interface while minimizing thermal management constraints. These findings indicate that the proposed topology offers a high-power-density and cost-effective solution for modern power electronic interfaces in bidirectional energy management systems.

Index Terms—Bidirectional multilevel inverter, Capacitive volt- age divider, Energy storage systems (ESS), Modified Nearest Level Control, Power quality, Seven-level inverter.

I. Introduction

The increasing integration of renewable energy sources and the growing demand for reliable energy storage systems (ESS) have driven significant advancements in power electronic converters. Multilevel inverters (MLIs) have emerged as a key technology for medium and high-power applications due to their ability to synthesize high-quality voltage waveforms with lower harmonic distortion, reduced voltage stress on switches, and smaller output filter requirements compared to conventional two-level inverters [1]–[3]. Typical MLI topologies such as Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB) are well-established, but they often suffer from drawbacks including a high number of isolated DC sources (CHB), complex capacitor voltage balancing (FC), or excessive clamping diodes (NPC) [4].

In many modern applications such as uninterruptible power supplies (UPS), electric vehicle (EV) charging stations, and residential or mobile energy storage units, bidirectional power flow capability is essential to allow both charging and dis- charging of batteries [5]. While several bidirectional MLI topologies have been proposed in the literature, they frequently require a large number of active switches, multiple isolated DC supplies, or intricate modulation schemes, which increase cost, size, and control complexity [6]–[9].

This paper introduces a novel 7-level bidirectional MLI topology that addresses these limitations. The key contributions of this work are:

- A single DC source combined with a capacitive voltage divider generates seven output voltage levels, eliminating the need for multiple isolated supplies.
- The topology uses only 13 switches (12 bidirectional and 1 unidirectional) and a single diode, resulting in a compact and cost-effective design.
- A Modified Nearest Level Control (NLC) strategy with pre-calculated switching angles ensures low harmonic distortion and inherent capacitor voltage balancing with- out high-frequency carrier signals or complex feedback loops.
- Simulation results at 5 kW demonstrate high efficiency (98.8% in inverter mode, 98.5% in rectifier mode) and an output voltage THD of 15%, confirming the effectiveness of the proposed solution for ESS and mobile power applications.

The remainder of this paper is organized as follows. Sec- tion II describes the proposed topology, its operating principle, and switching states. Section III presents the Modified NLC strategy. Section IV provides simulation results and performance analysis, including a comparison with existing topologies. Section V concludes the paper.

II. Proposed Topology and Operating Principle

A. Topology Description

Fig. 1 shows the power circuit of the proposed 7-level bidirectional MLI. The topology consists of a single DC voltage source V_{dc}, three series-connected capacitors C_1, C_2, C_3 acting as a voltage divider, 13 power switches S_1 to S_{13}, and one diode D_1. Switches S_1–S_{12} are bidirectional (imple- mented as back-to-back SiC MOSFETs) to allow current flow in both directions, while S_{13} is a unidirectional switch. The capacitor voltages are maintained at $V_{dc}/3$ each under ideal balanced conditions, providing intermediate voltage levels of $+V_{dc}$, $+2V_{dc}/3$, $+V_{dc}/3$, 0, $-V_{dc}/3$, $-2V_{dc}/3$, $-V_{dc}$. The component values used in this work are: $C_1 = C_2 = C_3 = 4700\ \mu$F (electrolytic type), and all switches are rated for appropriate voltage and current levels (1200 V, 50 A SiC MOSFETs).

Table I Switching States for the Proposed 7-Level Bidirectional MLI

Level	Output Voltage	Closed Switches
+3	$+V_{dc}$	S_1, S_2, S_3, S_{12}, S_{13}
+2	$+2V_{dc}/3$	S_1, S_2, S_3, S_8, S_9
+1	$+V_{dc}/3$	S_1, S_2, S_3, S_6, S_7
0	0	All switches are OFF
-1	$-V_{dc}/3$	S_8, S_9, S_{10}, S_{11}
-2	$-2V_{dc}/3$	S_6, S_7, S_{10}, S_{11}
-3	$-V_{dc}$	S_1, S_4, S_5, S_{10}, S_{11}

mode, power flows from the DC source to the AC load; in rectifier mode, power flows from the AC grid to the DC battery. The same switch states (Table I) are used in both modes, ensuring seamless transition. Fig. 2 shows the circuit configured for rectifier operation, where the AC source is connected to the output terminals and the DC side is connected to a battery or load.

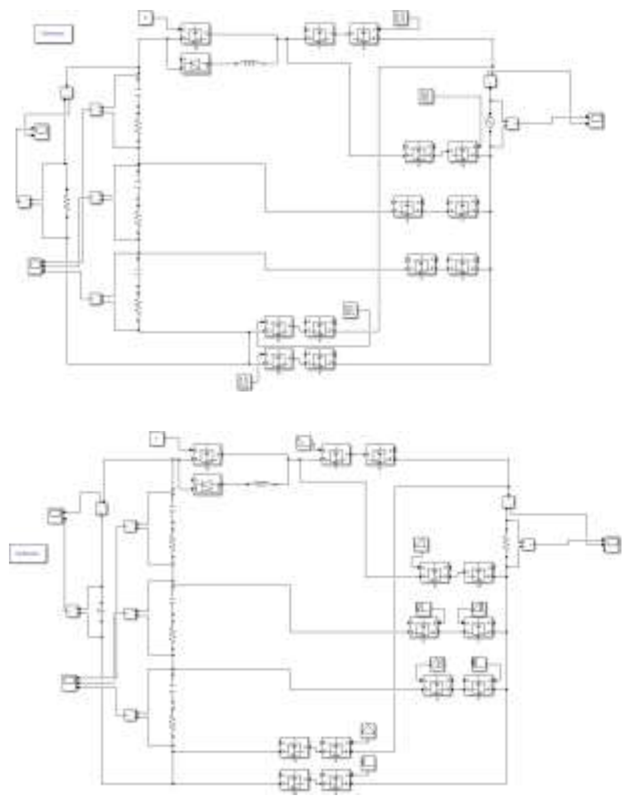

Fig. 1. Proposed 7-level bidirectional MLI topology (inverter mode configu- ration).

B. *Switching States and Level Generation*

Table I lists the switching states required to generate the seven output voltage levels. Each state corresponds to a specific combination of closed switches that connect the output terminal to the appropriate tap on the capacitor divider. The bidirectional nature of S_1–S_{12} allows the same states to be used for both inverter (DC→AC) and rectifier (AC→DC) operation, with only the direction of power flow reversed. Diode D_1 is only active in rectifier mode and does not conduct during inverter operation.

The capacitor voltages are inherently balanced due to the symmetric use of all three capacitors in each switching cycle. For example, during level $+V_{dc}$, capacitors C_2 and C_3 are in series with C_1 across the source, while at level $+V_{dc}/3$, only C_1 is used. This natural charge-discharge pattern prevents voltage drift without additional balancing circuits.

C. *Bidirectional Operation*

The topology supports bidirectional power flow by simply reversing the current direction through the switches. In inverter

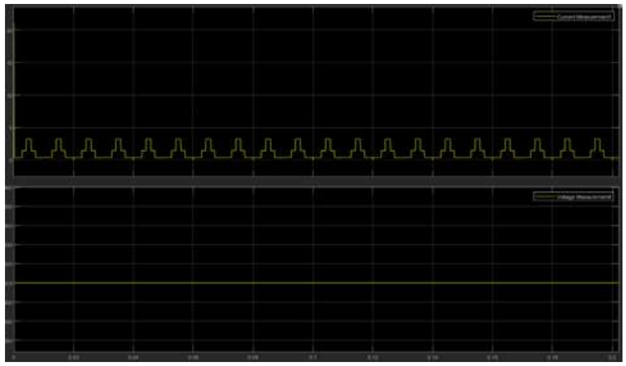

Fig. 2. Proposed topology in rectifier mode.

III. Modified Nearest Level Control Strategy

The proposed topology employs a simplified control ap- proach based on a Modified Nearest Level Control (NLC) strategy. Unlike conventional NLC methods that track a real- time reference voltage and select the nearest available level dy- namically, the proposed method utilizes pre-calculated switch- ing angles to generate the 7-level staircase waveform. This approach eliminates the need for high-speed processors, real-time feedback loops, or carrier-based modulation, significantly reducing computational complexity and cost.

A. *Switching Angle Calculation*

The switching angles ϑ_1, ϑ_2, ϑ_3 for the positive half-cycle of the output voltage are determined offline based on two primary objectives:

1) **Capacitor Voltage Balancing:** Maintaining the voltages across the three series capacitors C_1, C_2, C_3 at approx- imately $V_{dc}/3$ under steady-state conditions.
2) **Proper 7-Level Waveform Generation:** Ensuring that the output voltage exhibits seven distinct levels with correct polarity and step magnitudes.

To achieve capacitor voltage balance, the charge/discharge profile of each capacitor during each voltage level is ana- lyzed. The duration spent at each level (determined by the switching angles) is adjusted to ensure that all capacitors are equally utilized over a fundamental cycle. For example, during the highest positive level ($+V_{dc}$), capacitors C_2 and C_3 are discharged while C_1 is charged; at intermediate levels, different combinations of capacitors are involved. The angles are selected so that the net charge variation of each capacitor over one period is zero.

Table II Simulation Parameters

Parameter	Inverter Mode	Rectifier Mode
DC Side Voltage	325 V	300 V (output)
AC Side Voltage	230 Vrms (50 Hz)	230 Vrms (50 Hz)
Output Power	5 kW	5 kW
Load Resistance	10.58 Ω	18 Ω
Capacitors (C_1, C_2, C_3)	4700 μF each	4700 μF each
Switching Devices	SiC	MOSFET (1200V, 50A)
Switching Frequency	50 Hz	50 Hz
Control Method	Modified NLC	Modified NLC

This balancing condition is achieved by solving a set of equations that relate the switching angles to the capacitor volt- age variations. A trade-off is made by slightly compromising the output harmonic performance to maintain capacitor voltage balance and a clean 7-step waveform.

B. *Advantages and Trade-offs*

The key advantages of this control strategy are:

- Low computational burden: No real-time PWM genera- tion or reference tracking.

- No additional sensors: Capacitor voltages are not mea- sured, reducing cost.
- Simplified hardware: Suitable for low-cost microcon- trollers or even digital logic.

The main trade-off is a slightly higher output voltage THD (measured as 15% at full load in inverter mode) compared to optimized PWM methods. However, this level of distortion is acceptable for many energy storage and mobile power applications.

IV. Simulation Results

A. *Simulation Setup*

The proposed 7-level bidirectional MLI topology was mod- eled and simulated using MATLAB/Simulink environment to validate its performance in both inverter and rectifier operating modes. The simulation parameters are summarized in Table II.

B. *Inverter Mode Results*

Fig. 3 shows the input DC voltage and current waveforms. The DC input voltage is constant at 325 V, while the input current exhibits a pulsating nature corresponding to the output power delivery.

Fig. 4 presents the voltages across the three series capaci- tors C_1, C_2, C_3. The capacitor voltages remain well-balanced around $V_{dc}/3 \approx 108.3$ V throughout the operation, confirming the inherent balancing property achieved by the pre-calculated
switching angles. The small ripple is due to the charging and discharging cycles during each fundamental period.

Fig. 5 displays the output voltage and current waveforms. The output voltage clearly shows the expected 7-level staircase waveform with levels at +325 V, +216.7 V, +108.3 V, 0, -108.3 V, -216.7 V, -325 V. The output current is sinusoidal due to the resistive load, with a peak value of approximately 32.5 A (corresponding to 23 A rms). The measured total harmonic distortion (THD) of the output voltage at full load is 15%.

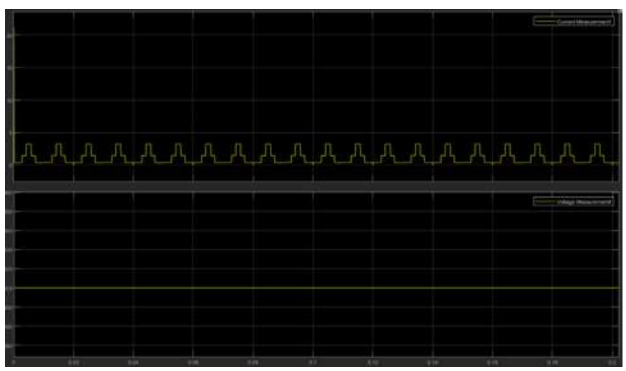

Fig. 3. Inverter mode: Input DC voltage (top) and current (bottom).

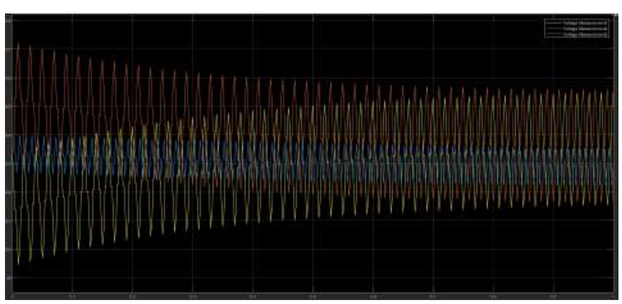

Fig. 4. Inverter mode: Capacitor voltage waveforms (C_1, C_2, C_3).

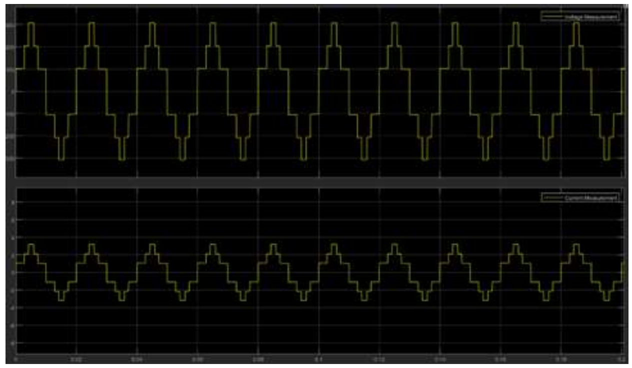

Fig. 5. Inverter mode: Output voltage (top) and current (bottom).

C. *Rectifier Mode Results*

Fig. 6 shows the AC input voltage and current waveforms in rectifier mode. The input voltage is a pure 230 Vrms, 50 Hz sinusoidal source, and the input current is nearly sinusoidal with a slight harmonic distortion due to the switching action. Fig. 7 presents the DC output voltage and current. The output voltage stabilizes at 300 V DC with low ripple, con- firming the rectifier operation. The output current is constant at 16.67 A for the 18 Ω load, delivering 5 kW to the DC side.

D. *Efficiency Analysis*

The efficiency of the proposed topology was evaluated at the rated 5 kW operating point for both modes. The input and output powers were measured, and the efficiency was calculated as:

$$\eta = Pout / Pin \times 100\% \qquad (1)$$

- Inverter mode: η = 98.8%
- Rectifier mode: η = 98.5%

These high efficiency values are attributed to the low switching frequency (50 Hz fundamental) and the use of SiC MOSFETs with low on-state resistance, minimizing both conduction and switching losses.

TABLE III Comparison of 7-Level Bidirectional MLI Topologies

Reference	THD (%)	Switch Count	Diode Count	Capacitor Count	Efficiency (%)	Switching Frequency	Bidirectional	Power Level
Siddique et al. [6]	–	11 (10+1)	0	5	97.7 (peak)	2.5 kHz	No	1.5 kW
Barzegarkhoo et al. [7]	–	11 (10+1)	0	6	97.4	20 kHz	No	1 kW
Baksi & Behera [8]	16.66	8 (6+2)	2	5	97.25	5 kHz	No	1 kW
Liu et al. [9]	23.86	8 (6+2)	0	5	–	10 kHz	No	310 W
Proposed Work	**15**	**13 (12+1)**	**1**	**3**	**98.8 / 98.5**	**50 Hz**	**Yes**	**5 kW**

Note: Some entries are left blank where data was not available.

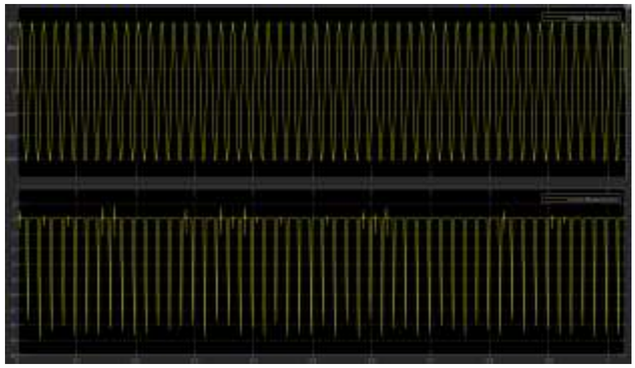

Fig. 6. Rectifier mode: AC input voltage (top) and current (bottom).

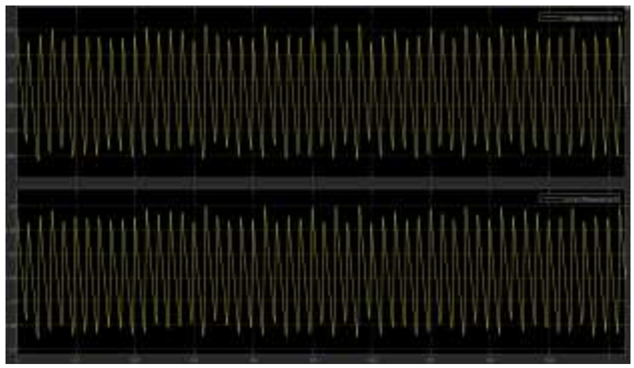

Fig. 7. Rectifier mode: DC output voltage (top) and current (bottom).

E. *Comparison with Existing Topologies*

Table III provides a comparative analysis of the proposed topology against existing 7-level bidirectional MLIs reported in the literature. The comparison considers key parameters including component count, THD, efficiency, and bidirectional capability.

The proposed topology offers several advantages:

- Highest efficiency among the compared converters (98.8% in inverter mode).
- True bidirectional operation enabling both inverting and rectifying modes.
- Reduced capacitor count (only 3) compared to many existing designs.
- Very low switching frequency (50 Hz) minimizing switching losses and electromagnetic interference.
- Single DC source requirement simplifying system integration.

F. Conclusion

This paper has presented a novel 7-level bidirectional mul- tilevel inverter topology designed for energy storage systems and mobile power applications. The proposed converter uti- lizes a single DC source with a capacitive voltage divider to generate seven output voltage levels, requiring only 13 switches (12 bidirectional, 1 unidirectional) and a single diode. A Modified Nearest Level Control strategy with pre-calculated switching angles ensures capacitor voltage balancing and proper 7-level waveform generation without complex real-time control or feedback sensors.

Extensive simulations at 5 kW rated power validated the topology's performance in both inverter and rectifier modes. The results demonstrate high efficiencies of 98.8% and 98.5% respectively, with an output voltage THD of 15% at full load. The capacitor voltages remain well-balanced throughout operation, confirming the effectiveness of the angle selection method.

Comparative analysis with existing 7-level bidirectional topologies shows that the proposed solution achieves superior efficiency, reduced component count, and true bidirectional capability while operating at fundamental switching frequency. These features make it an attractive candidate for cost-sensitive and high-power-density applications such as residential energy storage, UPS systems, and mobile power units.

Future work will focus on experimental validation through a laboratory prototype and investigation of closed-loop control strategies for grid-connected operation.

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