Uluslararası İleri Doğa Bilimleri ve Mühendislik Araştırmaları Dergisi
Sayı 7, S. 358-365, 4, 2023

Araştırma Makalesi

IJANSER
https://as-proceeding.com/index.php/ijanser
ISSN: 2980-0811

International Journal of Advanced Natural Sciences and Engineering Researches
Volume 7, pp. 358-365, 4, 2023

Research Article

An Improved Multi-Pulse Rectifier Circuit for Input Current Harmonic Suppression Using Passive Devices

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(Received: 20 April 2023, Accepted: 25 May 2023)

(DOI: 10.59287/ijanser.738)

(1st International Conference on Contemporary Academic Research ICCAR 2023, May 17-19, 2023)

ATIF/REFERENCE: Wahab, A., Khurshid, M. A & Mahmood, T. (2023). An Improved Multi-Pulse Rectifier Circuit for Input Current Harmonic Suppression Using Passive Devices. *International Journal of Advanced Natural Sciences and Engineering Researches*, 7(4), 358-365.

Abstract – Renewable energy resources, such as solar and wind, are increasingly being integrated into power systems to promote sustainable and clean energy generation. However, the intermittent nature of these resources poses challenges in terms of harmonics, power factor and power quality. This paper focuses on the use of multi-pulse rectifiers (MPR) as a solution for enhancing the performance and grid integration of renewable energy resources. A novel approach is introduced, combining a phase-shifting transformer that provides a five-phase input to a series of 20-pulse rectifiers with a pulse-tripling circuit (PPTC). By modulating the resultant currents of bridge rectifiers with PPTC, the rectifier's pulse number is raised from 20 to 60, resulting in enhanced reduction of input current harmonics. The proposed rectifier configuration achieves an input current with an approximate sinusoidal waveform, exhibiting a Total Harmonic Distortion (THD) of less than 4%. The proposed scheme offers several advantages. It is simple, utilizing only passive components without the need for active devices, making it easy to implement, improving the performance of rectifier, ensuring compliance with power quality standards, and enabling reliable operation in medium- and high-voltage electronic systems.

Keywords – Multi-Pulse Rectifier, Pulse-Tripling Circuit, Phase Shifting Transformer, Harmonic Reduction, Power Quality.

I. INTRODUCTION

The 12-pulse rectifier, which is arranged in series, is commonly utilized in medium- and high-voltage electronic devices to extract power from the electric grid. This enables the benefits of having a simple circuit configuration, being highly reliable, generating low EMI, and possessing a surplus capability [1]. However, the series-connected 12-pulse rectifier encounters issues with power quality such as injecting harmonics, rippled DC outputs, AC voltage disturbance and consequential in low power factor. Therefore, several standards have been recognized including the IEEE519 harmonic standards, which specify that a typical Total Harmonics Distortion (THD) of the input current larger than 10% does not fulfill the criteria. These

standards should be considered by designers, manufacturers, and users [2].

Numerous topologies have been suggested to effectively reduce the harmonics of input current of 12-pulse rectifier which is arranged in series [3]–[5]. There are two main approaches: the first involves installing filters such as active or passive power filters of the rectifier on the input side to suppress for the harmonics' input current [6], [7]. However, active filters are expensive and difficult to control, whereas passive filters have limited ability to suppress harmonics. The second technique involves increasing the frequency of diode rectifiers' pulses. According to studies on the use of 18- [8] and 20-Pulse Rectifiers [9], but they exhibit a Line current THD of over 5% with a light load or a low impedance source. A proposed 24-pulse rectifier [10] includes a secondary pulse-doubling circuit connected at its dc side. The pulse-doubling circuit modulation enhances the number of pulse from 12 to 24. The advantages of this technique are its simple implementation, high dependability, and simple circuit design. However, this scheme's harmonic suppression ability is constrained, and its input current THD remains below IEEE 519 standards. 36-pulse rectifier which is arranged in series using a five thyristors converter is presented [11]. The number of pulses can be amplified from 12 to 36 with the help of a five-thyristor converter to further reduce the rectifier's input current harmonics. The control of the rectifier is now more difficult and expensive due to the intricate nature of phase matching between thyristors and the requirement for five arrangements of trigger circuits and synchronization. Another option is to use three 36-pulse rectifiers connected in parallel with a pulse-tripling circuit, which modulates two rectifier bridges' output current and increases the equal amount of the output current [12]. This scheme is only suitable for medium and low voltage industrial applications, as in high- and medium-voltage applications, series connection of two 3-ϕ rectifier bridges are mostly used. The main disadvantage of this scheme is its limited applicability. Two passive voltage injection methods for rectifiers with 30 and 36 pulses are proposed, which indirectly reduce harmonics' input current to an adequate level [13], [14]. They indirectly lower the harmonics' input current to a adequate level while multiplying the pulse number to 30 or 36 of the rectifier's input voltage. However, because three high-capacity inductors must be linked on the input side in series, the output voltage characteristics of this scheme are smooth and easy to implement. In real-world applications, these techniques ought to be avoided. A passive harmonic reduction circuit for a 40-pulse DC link rectifier is suggested [15]. Despite being simple to implement, this scheme can only be used in low- and medium-voltage industrial applications.

In order to address the problems of the previously cited methods, a solution involving a phase shifting transformer providing a five-phase input to a series of 20-pulse rectifiers with a pulse-tripling circuit (PPTC) is proposed. This circuit includes a passive current forming network comprised of components C1, C2, and interphase reactor (IPR), as well as two auxiliary series reactors (ASRs) and a secondary 1-ϕ transformer (AST) with double secondary windings. The passive current forming network blocks the dc element in dc side's output voltage and creates a channel for alternating injection current. ASR1 modulates the rectifier bridges' output current of Rec1 and Rec2 directly in the load path in series connection. ASR2, on the other hand, modulates the rectifier bridges' resultant current of Rec1 and Rec2 indirectly with the load in parallel connection and varying based on the correlation between its input and load voltages. By simultaneously modulating ASR1 and ASR2, the voltage of Rec1 and Rec2 and output current are increased. This leads to an increase in the pulse number of the rectifier from 20 to 60 based on the voltage and current relationship on the DC and AC sides. The proposed approach modulates the bridge rectifier' output current and multiplies output current by changing conduction mode of secondary single-phase rectifier bridge. As a result, the pulse number of the rectifier's input current is raised to 60, further suppressing the input current harmonics. The proposed method offers several benefits. Firstly, it is simple and does not require active devices, making it easy to implement. Secondly, it utilizes only two small ASRs and a few passive components to achieve a 60-pulse rectifier from a 20-pulse rectifier, making it a inexpensive and efficient way for suppressing input current harmonics. Thirdly, it eliminates the need for large inductors of the rectifier on the input side, which can cause issues such as unbalanced output voltage and lowered displacement factor [14]. Overall, this scheme offers a straightforward and effective way to improve the performance of rectifiers.

II. MATERIALS AND METHOD

The article suggests an enhanced circuit design for Multi-Pulse Rectifier (MPR) aimed at suppressing input current harmonics. The proposed approach utilizes passive devices to address the issues mentioned above. The new topology includes a phase-shifting transformer that provides a five-phase input to a series-connected MPR, which is equipped on the DC side with a PPTC, as illustrated in Figure 1. The PPTC is responsible for regulating the resultant current of both rectifiers and increasing the amount of current by changing the diodes configuration linked to the non-traditional 1-φ rectifier bridges. By doing so, the rectifier's step

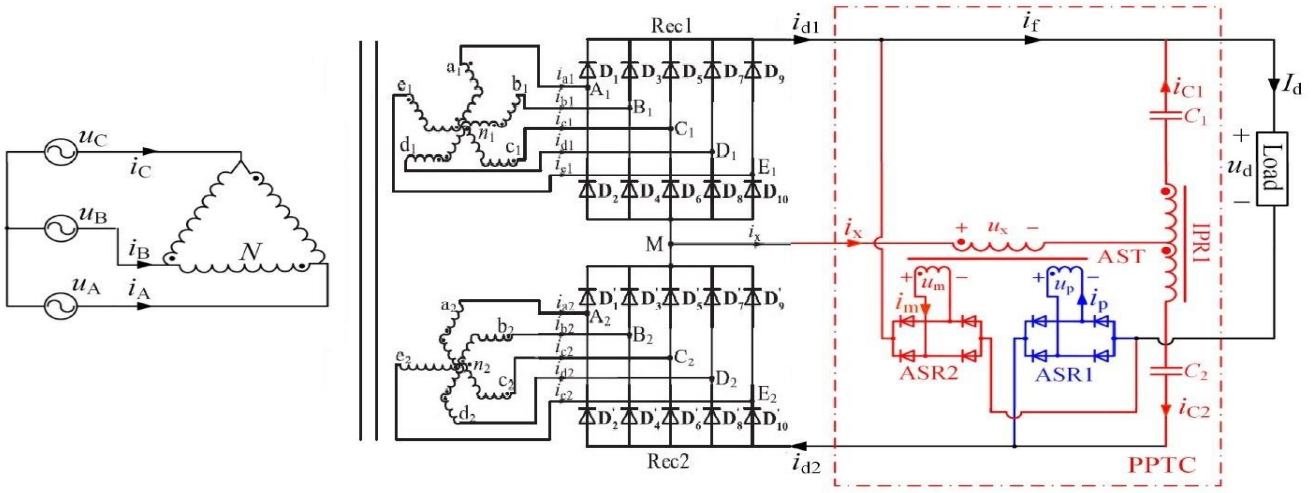

Fig. 1 Proposed Multi-Pulse Rectifier

count is increased to 60, resulting in enhanced suppression of harmonics in the input current.

A. *Designing Phase-Shifting Transformers*

The configuration of the 20-pulse rectifier involves the arrangement of two sets of diode bridge rectifiers (Rec1 and Rec2) that are connected in series and operate with a 5-ϕ input as depicted in Figure 2.

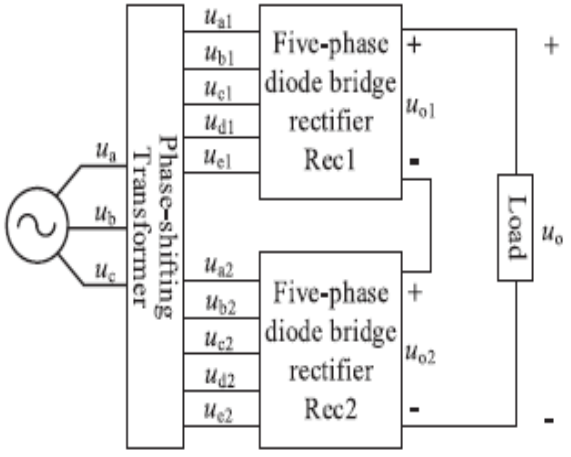

Fig. 2 The 20-pulse rectifier

To ensure the proper operation of both rectifiers in the circuit of MPR (Multi-pulse Rectifier), it is necessary to maintain a specific phase difference ϑ between the multiple sets of output voltages generated by the phase-shifting transformer must be in accordance with the rectification principle.

$$\vartheta = \frac{360^\circ}{M_1 M_2} \qquad (1)$$

Where M1 represents the quantity of output pulses generated by each bridge rectifier, while M2 denotes the number of bridge rectifiers.

According to Figure 2 and equation (1), both sets of 5-φ output voltages must fulfill certain conditions: they must have the equal root-mean-square (rms) value, and their phase difference ϑ should be 18°. To enhance the protection of the rectifier, a fully isolated phase-shifting transformer is developed, as illustrated in Figure 2. Windings at primary side are connected in delta, whereas windings at secondary side are connected in two groups of zigzag. Figure 3 shows the phasor diagram of the phase-shifting transformer. The input voltage phasors exhibit a phase difference of 120°, whereas the first group of 5-φ output voltage phasors show a phase difference of 72°. The phasors of the second group of 5-φ output voltages are 18° behind the phasors of the first group of 5-φ output voltages.

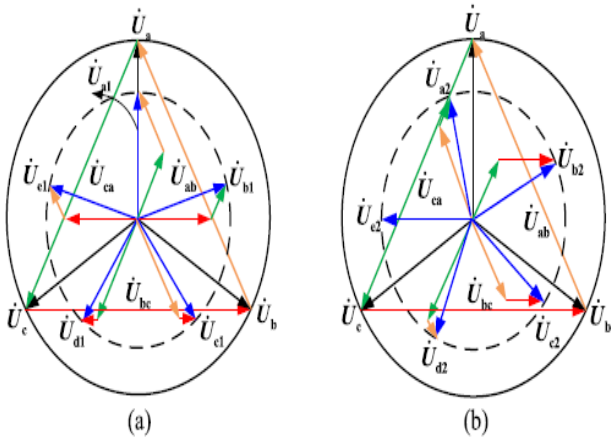

Fig. 3 Phase shifting transformer's phasor diagram. (a) First group of output voltages' phasor diagram. (b) Second group of output voltages' phasor diagram.

It is possible to calculate the relationship between each phasor's rms value from Figure 3. The phasor $\dot{U_{a1}}$ can be expressed as:

$$\dot{U_{a1}} = -K_1\dot{U_{ca}} + K_2\dot{U_{ab}} \quad (2)$$

The proportional coefficients between the secondary winding and primary winding are denoted as K1 and K2. These coefficients can be determined using the Law of Sines.

$$K_1 = K_2 = \frac{\sin 30°}{\sqrt[3]{3}\,K \sin 120°} \quad (3)$$

The variable K denotes the rms voltage fraction of the input and output of the phase-shifting transformer.

B. *The proposed Multi-Pulse Rectifier*

In Figure 1, a Multi-Pulse Rectifier (MPR) circuit with a dc side PPTC is shown. The MPR consists of two series connected 5-ϕ diode bridge rectifiers. Additionally, the PPTC comprises two ASRs, a 1-ϕ transformer with dual secondary winding, and a passive current forming network.

The optimal turns ratio of the 1-ϕ transformer connected to the bridge rectifier is determined through a calculation process.

The rectifier's 3-φ input voltage is represented as follows:

$$u_A = \sqrt{2}E\sin(\omega t) \quad (4)$$
$$u_B = \sqrt{2}E\sin(\omega t - 2\pi/3) \quad (5)$$
$$u_C = \sqrt{2}E\sin(\omega t + 2\pi/3) \quad (6)$$

The variable E represents the rms value of the input voltages.

The determination of the output voltage of the phase-shifting transformer is based on the correlation between its primary and secondary windings are as follows:

$$u_{a1} = \sqrt{2}KE\sin(\omega t) \quad (7)$$
$$u_{b1} = \sqrt{2}KE\sin(\omega t - 2\pi/5) \quad (8)$$
$$u_{c1} = \sqrt{2}KE\sin(\omega t - 4\pi/5) \quad (9)$$
$$u_{d1} = \sqrt{2}KE\sin(\omega t + 4\pi/5) \quad (10)$$
$$u_{e1} = \sqrt{2}KE\sin(\omega t + 2\pi/5) \quad (11)$$

$$u_{a2} = \sqrt{2}KE\sin(\omega t + \pi/10) \quad (12)$$
$$u_{b2} = \sqrt{2}KE\sin(\omega t - 3\pi/10) \quad (13)$$
$$u_{c2} = \sqrt{2}KE\sin(\omega t - 7\pi/10) \quad (14)$$
$$u_{d2} = \sqrt{2}KE\sin(\omega t + 9\pi/10) \quad (15)$$
$$u_{e2} = \sqrt{2}KE\sin(\omega t + 5\pi/10) \quad (16)$$

The value of K represents the ratio between the input and output rms voltages of the phase-shifting transformer.

Using this relationship, the output voltage of the 3-φ rectifiers, Rec1 and Rec2, can be calculated as:

$$u_{d1} = u_{a1}S_{a1} + u_{b1}S_{b1} + u_{c1}S_{c1} + u_{d1}S_{d1} + u_{e1}S_{e1} \quad (17)$$

$$u_{d2} = u_{a2}S_{a2} + u_{b2}S_{b2} + u_{c2}S_{c2} + u_{d2}S_{d2} + u_{e2}S_{e2} \quad (18)$$

The variable S_{u1} denotes the state of conduction of the a1-phase of Rec1 and represents the corresponding switching function between currents i_{a1} and i_{d1}.

The load voltage equation is fulfilled in Figure 1.

$$u_d = u_{d1} + u_{d2} \quad (19)$$

Relationship for u_z in Fig.1 can be obtained as

$$u_z = \frac{1}{2}(u_{d2} - u_{d1}) \quad (20)$$

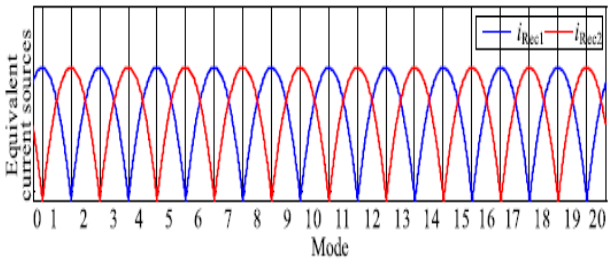

Fig. 4 Current of waveform i_{d1} and i_{d2}.

Figure 4 illustrates the waveforms of i_{d1} and i_{d2} currents, both having the same root mean square (rms) value and a phase angle difference of 18°. The diodes in each rectifier conduct for 72° per power cycle, and there is always a conducting diode on both the lower and upper bridge arms of each rectifier at any given time.

C. PPTC Operating Stages

The PPTC has four operating stages, namely Stage 1, Stage 2, Stage 3, and Stage 4, based on the working conditions of ASR1 and ASR2. The operating Stages of the rectifier are illustrated in Figure 5.

Stage 1: When $u_p > 0$ and $u_m < u_d$

ASR2 remains non-conductive as all diodes in it are reverse-biased. Therefore, the input current i_m in ASR2 is zero. Meanwhile, diodes D_{p2} and D_{p3} in ASR1 are switched on, allowing the output current i_d to flow through them and supply electric power to the load. This happens because the voltage $u_p > 0$.

$$i_{d1} = (1 - \frac{p}{2})I_d \quad (21)$$

$$i_{d2} = (1 + \frac{p}{2})I_d \quad (22)$$

$$u_d = u_{d1} + u_{d2} + \frac{p}{2}(u_{d2} - u_{d1}) \quad (23)$$

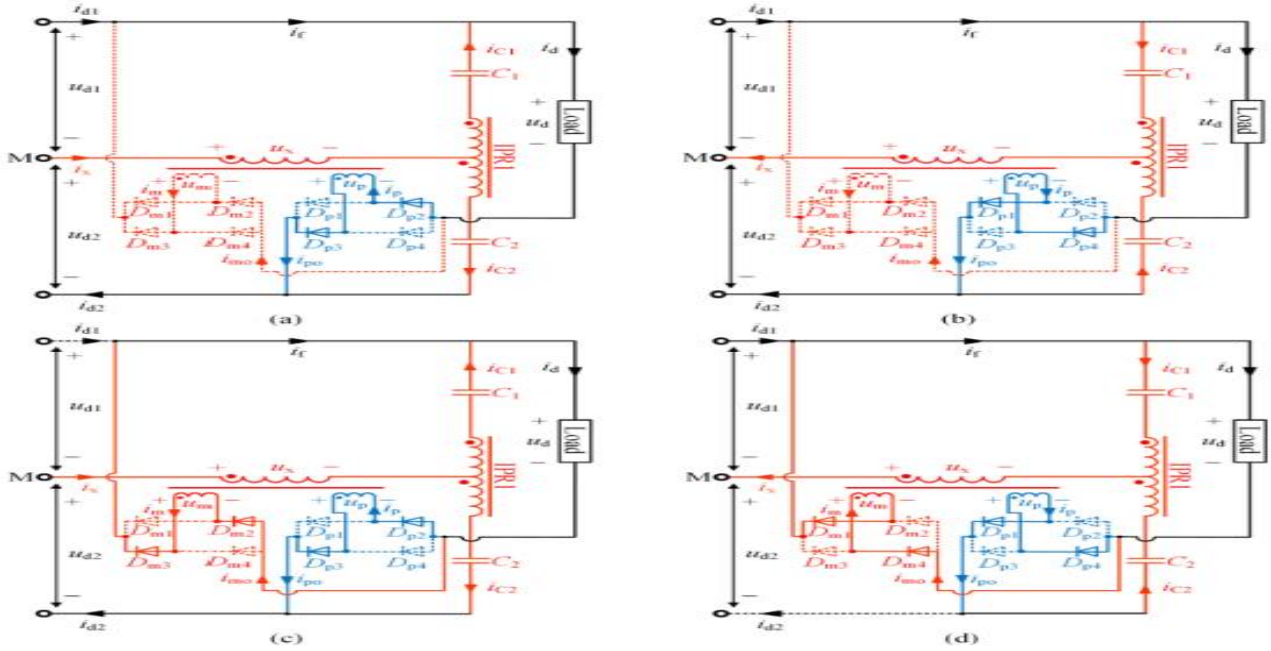

Fig. 5 PPTC Operating Stages. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4.

Stage 2: When $u_p < 0$ and $u_m < u_d$

ASR2 remains inactive with all diodes reverse biased, resulting in a zero-input current i_m. Diodes D_{p1} and D_{p4} in ASR1 are turned on as $u_p < 0$, allowing the output current i_d of the rectifier to flow through them and supply power to the load.

$$i_{d1} = (1 + \frac{p}{2})I_d \quad (24)$$

$$i_{d2} = (1 - \frac{p}{2})I_d \quad (25)$$

$$u_d = u_{d1} + u_{d2} - \frac{p}{2}(u_{d2} - u_{d1}) \quad (26)$$

Stage 3: When $u_p > 0$ and $u_m > u_d$

During this operating Stage, the diodes D_{m2} and D_{m3} in ASR2 are forward biased and conductive, allowing an input current i_m to flow. The diodes D_{p2} and D_{p3} in ASR1 are switched ON, resulting in input current of ASR1 $i_p > 0$ because $u_p > 0$. As a result, the diodes in Rec1 become reverse biased and do not conduct, while the diodes in Rec2 become forward biased and conduct, causing the output current i_{d1} to flow in the forward direction. Thus, power is supplied to the load by both Rec2 and ASR2 together.

$$i_{d1} = 0 \quad (27)$$

$$i_{d2} = \frac{2m}{m-p+2} I_d \quad (28)$$

$$u_{d1} = \frac{m-p-2}{m-p+2} u_{d2} \quad (29)$$

$$u_d = \frac{2m}{m-p+2} u_{d2} \quad (30)$$

Stage 4: When $u_p < 0$ and $-u_m > u_d$

During this Stage, diodes D_{m1} and D_{m4} in ASR2 become forward biased and conductive. The input current of ASR2, denoted as $-i_m$, is greater than 0. Diodes D_{p2} and D_{p3} in ASR1 are turned ON, and the input current of ASR1 is $-i_p > 0$ since $u_p < 0$. The diodes in Rec2 are reverse biased, and its output current, denoted as i_{d2}, is 0. On the other hand, the diodes in Rec1 become forward biased, and its output current, i_{d1} is greater than 0. As a result, both Rec1 and ASR2 contribute to supplying power to the load.

$$i_{d1} = \frac{2m}{m-p+2} I_d \quad (31)$$

$$i_{d2} = 0$$

$$u_{d2} = \frac{m-p-2}{m-p+2} u_{d1} \quad (32)$$

$$u_d = \frac{2m}{m-p+2} u_{d1} \qquad (33)$$

The PPTC modulation strategy enhance the output levels of Rec1 and Rec2 initially and then enhance the number of pulses of the rectifier based on the current correlation between the AC and DC sides and the voltage correlation on the DC side.

Table 1. Simulation Parameters

Parameters	Values
Input Voltage (V_{rms})	220 V
Frequency	50 Hz
Load	80 Ω
Proportional coefficient (K)	(3:1)
AST Turn Ratio	1:42.98:0.653
Filter Inductance	15 mH

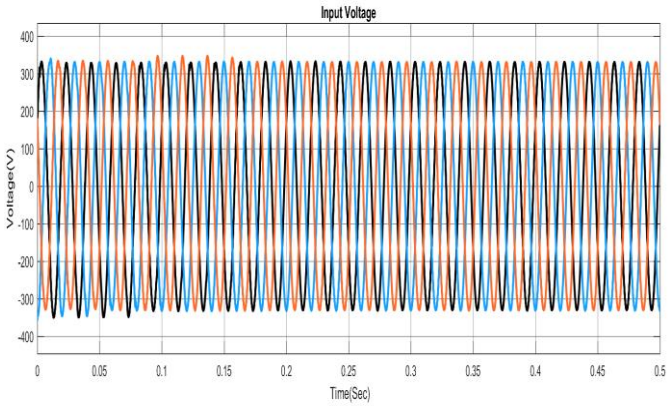

Fig. 6 Phase shifting Transformer's Input Voltage

III. RESULTS

The simulation results presented in this article validate the effectiveness of the proposed scheme. The Parameters for simulation are presented in Table I. The input voltage of the phase-shifting transformer is illustrated in Figure 6, where the dominant harmonic corresponds to the (60k±1)th harmonic with THD of 3.6% in the input supply. Here, "k" represents a positive number. Figure 7 illustrate the 60-pulse rectifier's input current, which consists of 60 arcs during a power cycle. In the absence of the PPTC, the rectifier operates conventionally as a series-connected 20-pulse rectifier. The input current consists of 20 steps and is predominantly characterized by harmonics of the 19th and 21th orders. When the PPTC is implemented, the input current undergoes a transformation, expanding it to 60 steps. This increase in steps leads to a higher level of precision, effectively reducing and nearly eliminating the presence of harmonics such as the 19th, 21th, 29th, 31th, 39st, and 41th order harmonics in the input current. The simulation results indicate a total harmonic distortion value of 1.19%. The rectifier load is approximately 1.5 kW, considering the rms values of the load.

IV. DISCUSSION

The proposed circuit design provides an effective solution for suppressing input current harmonics in Multi-Pulse Rectifiers. In the 5-phase rectifiers, each diode remains on for 72° in one cycle, and there is an 18° phase difference between phases "a1" and "a2". This confirms that PPTC does not affect the operational modes of 5-ϕ bridge rectifiers. To validate the effectiveness of the proposed design, extensive analysis and experimental results would been provided. Further research and practical implementation of this design can contribute to the improvement of power quality and the reliable operation of electronic systems in various applications.

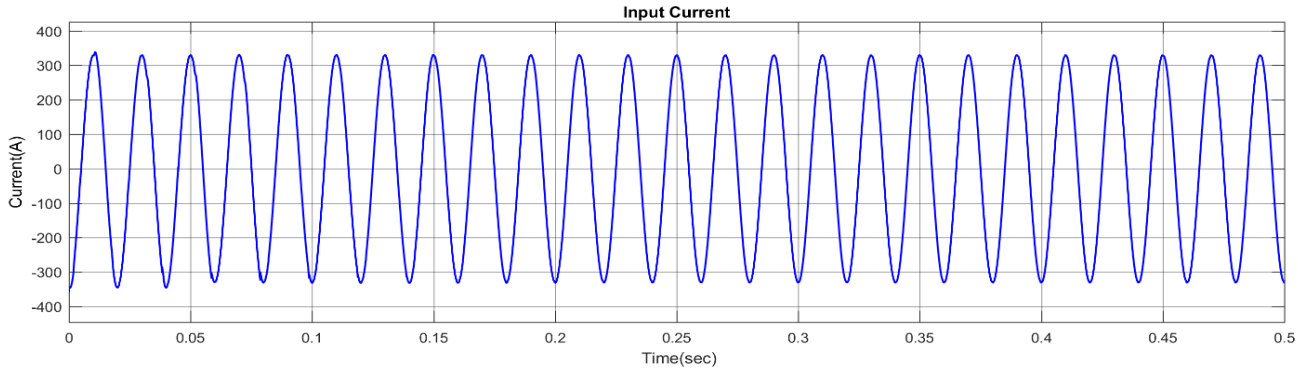

Fig. 7 Input Current of Multi-Pulse Rectifier

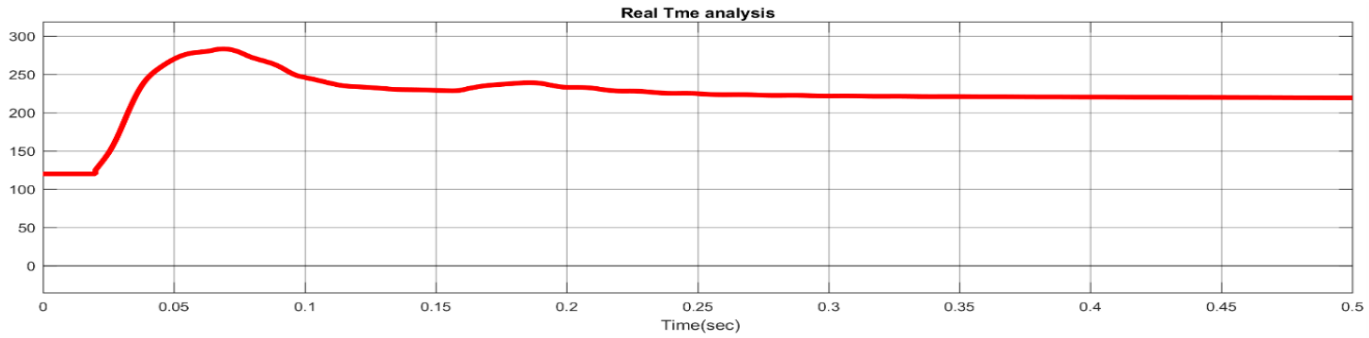

Fig. 8 Real-time Harmonic Suppression

V. CONCLUSION

The proposed topology ensures compliance with power quality standards and enables the smooth operation of medium- and high-voltage electronic systems by incorporating a phase-shifting transformer and a Pulse-Tripling Circuit (PPTC), the rectifier's step count is increased to 60, resulting in enhanced suppression of harmonics' input current. The PPTC modulation strategy employed in the proposed scheme effectively enhances the resultant levels of the rectifier bridges (Rec1 and Rec2) and enhances the number of pulses of the rectifier based on the correlation between the AC and DC currents and the voltage on the DC side. The resulting input current waveform approximates a sinusoidal shape with THD of less than 4%. This article has exhibited an innovative circuit design for Multi-Pulse Rectifiers (MPRs) to effectively suppress input current harmonics. The proposed approach utilizes passive components, offering a cost-effective and reliable solution.

ACKNOWLEDGMENT

The author extends his sincere appreciation to Prof. Dr. Tahir Mahmood (Department of Electrical Engineering, U.E.T Taxila) for his valuable assistance in the selection of the case for this study. The author is grateful to the referees for their valuable comments and suggestions, which have proven to be highly beneficial for the improvement of this work.

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