Uluslararası İleri Doğa Bilimleri ve Mühendislik Araştırmaları Dergisi
Sayı 7, S. 14-20, 6, 2023
© Telif hakkı IJANSER'e aittir
Araştırma Makalesi

IJANSER

https://as-proceeding.com/index.php/ijanser
ISSN: 2980-0811

International Journal of Advanced Natural Sciences and Engineering Researches
Volume 7, pp. 14-20, 6, 2023
Copyright © 2023 IJANSER
Research Article

ASIC vs FPGA based Implementations of Built-In Self-Test

Afaq Ahmad[1]*, Sabir Hussain[2], M A Raheem[3], Ahmed Al Maashri[4], Sayyid Samir Al Busaidi[5] and Medhat Awadalla[6]

[1]*Department of Electrical & Computer Engineering, Sultan Qaboos University, Oman*
[2, 3]*Department of Electronics and Communication Engineering, M. J. College of Engineering and Technology, Osmania University, Hyderabad, India*
[4, 5, 6]*Department of Electrical & Computer Engineering, Sultan Qaboos University, Oman*

*(afaq@squ.edu.om)

(Received: 29 June 2023, Accepted: 13 July 2023)

ATIF/REFERENCE: Ahmad, A., Hussain, S., Raheem, M. A., Maashri, A. A., Busaidi, S. S. & Awadalla, M. (2023). ASIC vs FPGA based Implementations of Built-In Self-Test. *International Journal of Advanced Natural Sciences and Engineering Researches*, 7(6), 14-20.

Abstract – Linear Feedback Shift Registers (LFSRs) are play key role in testing of for Very Large Scale Integration (VLSI) Integrated Circuits (ICs) testing. Due to tremendous IC complex growth, testing of recent VLSI ICs technology have become more complicated. This led to develop a popular alternate viable solution in the form of Built-In Self-Test (BIST) technology as compared to Automatic Test Equipment (ATE). However, the challenges of BIST technology remain the subject of research. Furthermore, implementation of BIST's LFSR on Application Specific Integrated Circuit (ASIC) versus Field Programmable Gate Array on (FPGA) platform is current area of research especially in context to power consumption. Hence, to make an informed choice between ASIC and FPGA for implementing BIST's LFSR we focus on study of design of reconfigurable LFSR on ASIC versus FPGA platform. The Electronic Design Automation (EDA) tool, Cadence is used for implementing BIST's LFSR on ASIC platform. Whereas, Hardware Description Language (HDL), Verilog is used to implement BIST's LFSR on FPGA platform. During experimental methodology, maximum frequency, the critical path delay is investigated to assess the power dissipation. The functional and timing simulation models are used to verify the implemented reconfigurable BIST's LFSR designs. The obtained results show that the performance, in terms of speed and power, of ASIC implementation is far better than traditional FPGA implementation.

Keywords – FPGA, ASIC, BIST, LFSR, Power Dissipation, Bit Swapping

I. INTRODUCTION

The main challenging areas in VLSI testing are performance, cost and power dissipation. There exist solutions for performance and cost such as Design for Testability (DFT), Built-In Self-Test (BIST). However, power dissipation, the power consumed during testing is due to switching activity pose great challenge for DFT and BIST. Furthermore, the demand for portable computing devices and communications system are increasing rapidly. These portable devices are generally designed around ASIC and FPGA. The test application time as the test has to run for longer time to reach sufficient fault coverage, in turn increase in power and test time [1, 2].

Various methods have been proposed to tackle the power dissipation problem during testing. In a research work [3], to reduce the power dissipation, a BIST Test Pattern Generator (TPG) design is suggested to reduce the power via controlling and maintain low switching activity. The new proposed Automatic TPG (ATPG) algorithm succeeded to reduce average heat dissipation between successive test vectors. Using the bit swapping technique, researchers [4] proposed the modified design of Linear Feedback Shift Register (LFSR), which is an integral part of BIST and abled to reduce the number of transitions at the input Circuit under Test (CUT) by 25 percent.

Through experimental results on ISCAS'85 and ISCAS'89 benchmark circuits, the research work have been demonstrated the reduction of power up to 45 percent during testing process. The researchers [5] have also shown that the proposed design can be combined with other techniques to achieve a very substantial power reduction up to a level of 63 percent. Further, the researchers proposed a design for memory BIST with feature of low power address generator. Using LFSR as address generator, they succeeded to achieve around 60 percent reduction in switching activity. They designed the address decoder for large address spaces with negligible overhead in hardware area.

A Low Transition (LT) BIST pattern generator called LT-LFSR, to reduce average and peak power of a circuit during test by reducing transitions within random test patterns and between consecutive patterns have been proposed [6]. The proposed LT-LFSR reduced transitions by inserting intermediate vectors between two consecutive vectors generated by the LFSR. This work was carried out on the centered idea of combining properties of two different LFSRs, the Bipartite LFSR and the Random Bit Injection (RBIJ) LFSR.

An idea of ASIC vs FPGA implementation of LFSR on cryptography systems using ciphering technology have been investigated by researchers [7]. Continuing the research ahead we researched and propose a low power LFSR, which uses bit swapping technique to reduce the power in test mode of the BIST operation. Using the proposed LFSR structuring model, we studied to investigate ASIC versus FPGA based implementations of BIST suitability.

II. Background Knowledge

In this section, we present the necessary background knowledge related to the research.

A. *Power Dissipation*

The dominant factor in dynamic power dissipation, which is proportional to the square of the supply voltage, arises from transient switching behavior of the nodes. The transition back and forth between the two logic levels, resulting in the charging and discharging of parasitic capacitances in the circuit. In digital circuits, the sources of average power consumption (P_{av}) are categories as below and illustrated by Equation (1).

- Static power dissipation (P_{st}),
- Short-circuit power dissipation (P_{sc}), and
- Dynamic power dissipation (P_{dv}).

$$P_{av} = P_{st} + P_{sc} + P_{dv} \quad (1)$$

Static power dissipation occurs when the logic gate output is stable hence, P_{st} is frequency independent. Complementary Metal Oxide Semiconductor (CMOS) devices have very low-static power dissipation and most of the energy in them is used to charge and discharge load capacitances as shown in Equation (2). Short-circuit power dissipation occurs when current flows from power supply (V_{dd}) to ground (GND) during switching. The value of P_{sc} depends on the amount of short circuit current flowing to GND; refer to Equation (3).This virtual world is becoming reality for most of the people in the world and in that way the importance of information security becomes equivalent to physical protection in the real world.

$$P_{st} = V_{dd} I_{leakage} \quad (2)$$

$$P_{sc} = V_{dd} I_{short\ circuit} \quad (3)$$

In CMOS devices, P_{dv} is the dominant source of power dissipation and accounts for approximately 90 percent of P_{dv}. Dynamic power dissipation occurs during the switching of logic gates and hence, P_{dv} is frequency dependent. As given in Equation (4), P_{dv} is therefore, the average power required to perform all the switching events across the circuit.

$$P_{dv} = \beta\, C_0\, V_{dd}^2\, f \quad (4)$$

Where β is switching activity per node. C_0 is switched capacitance and f is frequency, i.e. switching events per second.

To evaluate P_{dy}, which is the sum of transient power consumption (P_{tr}) and capacitive load power consumption (P_{ca}). Where, the value P_{tr} represents the amount of power consumed when the device changes logic states, i.e. 1 bit to 0 bit or vice versa and the value of P_{ca}, represents the power used to charge the load capacitance (Cleakage). Together we find that

$$P_{dy} = P_{ca} + P_{tr} = (C_{leakage} + C)V_{dd}^2 . fN^3 \quad (5)$$

Where C is the internal capacitance of the IC and N is the number of bits that are switching.

B. *Built-In Self-Test*

Design for Testability (DFT) is a technique using which the circuit designed in such a way that it becomes easy to test. This is done by increasing the circuit observability and controllability, which directly increases the testability of the circuit. Observability is defined as the difficulty of observing internal circuit lines at primary outputs. Controllability is defining as the difficulty of setting internal circuit lines to 0 or 1 from primary inputs. Built in Self-Test (BIST) one of the most used DFT technique.

Built-in self-test is a structural test method, which adds test logic circuit to an IC that allows the IC to test its own operation during test mode. Logic BIST consists of Pseudo-Random (PR) TPG to generate input patterns that are applied to internal scan chains. The response from the CUT are compressed into a signature through a Multi-Input Signature Register (MISR). Then, comparison of obtained signature with fault-free signature determines whether the fault exist or not to tell if all tests passed. The basic structure of BIST is shown in Figure 1.

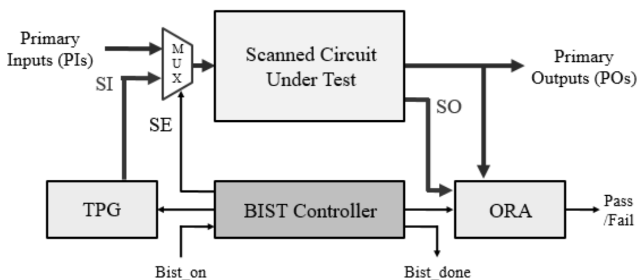

Fig. 1. A typical BIST structure

Circuit Under Test (CUT), usually using full-san DFT. The BIST Controller is to produce control signal. Test Pattern Generator (TPG), generates test pattern to Scan-In (SI).

Through Output Response Analyzer (ORA), fault-free value compared to Primary Outputs (POs) and Scan Output (SO).

Typically, by adding a test mode to the circuit and all flip-flops functionally form one or more shift registers called scan chains. Scan chains have a unique scan-input per scan segment. Thus, the length of scan chains is equal to the number of scan flip-flops divided by the number of scan inputs specified by the designer. Figure 2 shows a scan design schematic.

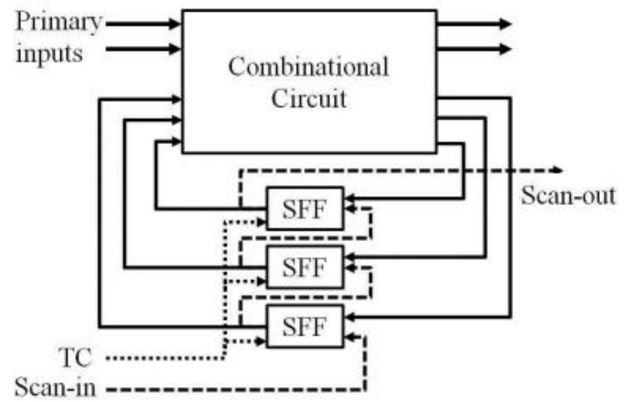

Fig. 2. A scan design schematic

Scan design can operate in three modes:

- Normal mode,
- Shift mode, and
- Capture mode.

In the normal mode, all test signals are turned off, and the scan design operates in the normal functional configuration mode. In both shift mode and capture mode, using a Test-mode Control signal (TC), all flip-flops can be set to any desired states by shifting those logic states into the scan chain. Similarly, the captured test responses stored in flip-flops can be observed by shifting the contents of the scan chain out. The most widely used scan cell is Multiplexed-D Flip-Flop (FF) as shown in Figure 3. The multiplexer uses a Scan Enable (SE) input to select between the Data-In (DI) and the SI.

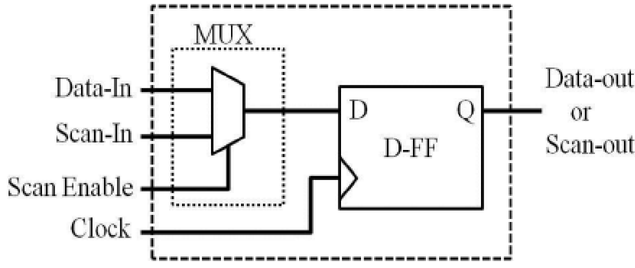

Fig. 3. A multiplexed D-cell scan

III. Methodology and Method

Built-in self-test that implements its pseudo-random TPG and MISR using LFSR has been proven as one of the most cost-effective and widely used solutions for VLSI circuit testing [1].

In our experiment we use a low power consumed LFSR, which uses bit-swapping technique to reduce the power in test mode [8]. As shown in Figure 4, an LFSR consists of two parts; A Shift Register (SR) and a feedback function. The LFSR consumes large amount of power during testing mode.

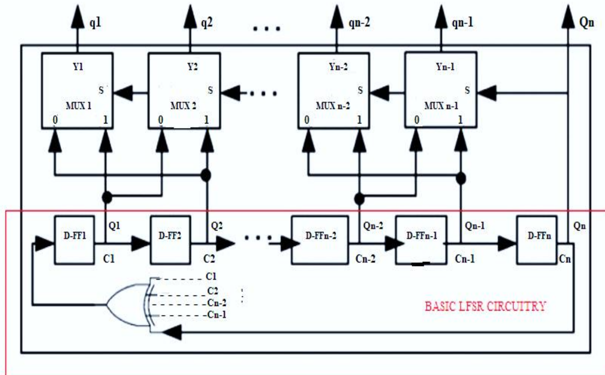

Fig. 4. Modified BIST structure used in experimental setup

Equation (6) describes the model of the LFSR shown in Figure 2, where the state of the LFSR at any time‘t’ be represented by vector$[Q(t)] = [Q1(t), Q2(t), \ldots Qn-2(t), Qn-1(t), Qn(t)]$.

$$\begin{bmatrix} Q_1(t+1) \\ Q_2(t+1) \\ \vdots \\ Q_{n-1}(t+1) \\ Q_n(t+1) \end{bmatrix} = \begin{bmatrix} C_1 & C_2 & C_3 & \cdots & C_{n-1} & C_n \\ 1 & 0 & 0 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \cdots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & 0 & 0 \\ 0 & 0 & 0 & \cdots & 1 & 0 \end{bmatrix} * \begin{bmatrix} Q_1(t) \\ Q_2(t) \\ \vdots \\ Q_{n-1}(t) \\ Q_n(t) \end{bmatrix}$$

(6)

Where, $C_j = 0 \; or \; 1$ for$1 \le j \le n-1$, and

$$C_j = 1, \text{for } j = n. \tag{7}$$

Equation (6) can be written as

$$[Q(t+1)] = [A]\,[Q(t)] \tag{8}$$

Based on the property of periodicity of LFSR and Equation (8), it follows that

$$[Q(t)] = [Q(t+p)] = [A]^P [Q(t)] \tag{9}$$

Assertion 1: [9 -12]

The period p of an n-bit LFSR will only be maximal when $p = m = 2^n - 1$.

Definition 1:

For the state matrix A of LFSR, the characteristic polynomial $\varphi(x)$ is given by Equation (10)

$$\varphi(x) = 1 + \sum_{j=1}^{n} C_j\, x^j \quad C_n = 1. \tag{10}$$

In our experiment, an n-bit maximal LFSR is considered. Using 2x1 MUX and maximal LFSR, bit-swapping LFSR is constructed. As shown in Figure 4, the final state vectors are recorded as:

$$[q(t)] = [q_1(t), q_2(t), \ldots, q_{n-2}(t)\; q_{n-1}(t), Q_n(t)].$$

As an example, let us consider n = 5 and the characteristic polynomial $\varphi(x) = 1 + x^3 + x^5$.

The generated test sequence vectors for both, maximal LFSR and bit-swapping scheme are as given below through Table 1. In the table, the mentioned states are presented in hexadecimal value (*0x*). The states of the maximal LFSR and Bit-swapping LFSRs are computed using a developed algorithm.

It can be verified that the states of maximal LFSR will switch to the following states.

0x01- 0x10 - 0x08 - 0x04 - 0x12 - 0x09 - 0x14 - 0x1A - 0x0D - 0x06 - 0x13 - 0x19 - 0x1C - 0x1E - 0x1F - 0x0F - 0x07 - 0x03 - 0x11 - 0x18 - 0x0C - 0x16 - 0x1B - 0x1D - 0x0E - 0x17 - 0x0B - 0x15 - 0x0A - 0x05 - 0x02 - 0x01.

From the Table 1 it can be analyzed that for the generated test sequence length of period 31 cycles (2^n*-1*), there exists 16 transitions per bit for each Q_1, Q_2, Q_3, Q_4 and Q_5 vectors. Whereas, the transitions

per bit for each q_1, q_2, q_3 and q_4 is reduced to 12 i.e. reducing the switching activity by 25 percent.

IV. Simulation Study

Shown in Figure 5, is the schematic view of maximal LFSR, which is executed on Cadence RTL Compiler. There are number of buffers (as D-FFs) whose outputs are connected to each other internally. Finally, all the outputs of the LFSR cells are stored and stream of bits are generated as test vector, TPG.

To validate the effectiveness of the proposed approach we select traditional LFSR technique for simulation and synthesis, which were carried out with Cadence Sim-Vision and Cadence RTL Compiler GPDK 180 nm. CMOS library is used We also carried the same design in FPGA targeting on Spartan 3E to validate clock frequency to compare with ASIC design.

Table 1. The state diagrams for maximal LFSR and bit swapper LFSR ($\varphi(x) = 1 + x^3 + x^5$).

Clk	Maximal LFSR 0x[Q_1, Q_2, Q_3, Q_4, Q_5]	Bit-swapped LFSR 0x[q_1, q_2, q_3, q_4, Q_5]
1	01	01
2	10	08
3	08	10
4	04	02
5	12	0C
6	09	09
7	14	0A
8	1A	1C
9	0D	0D
10	06	06
11	13	13
12	19	19
13	1C	1A
14	1E	1E
15	1F	1F
16	0F	0F
17	07	07
18	03	03
19	11	11
20	18	18
21	0C	12
22	16	0E
23	1B	1B
24	1D	1D
25	0E	16
26	17	17
27	0B	0B
28	15	15
29	0A	14
30	05	05
31	02	04
32	01	01

	Total Transition 16+16+16+16+16 = 80	Total Transition 12+112+12+112+16 = 64

In our experimental setup, we considered post layout simulation of maximum LFSR. The test patterns are generated using the LFSR, which is described in Verilog HDL code.

We used, 16 bit, ISCAS' 85 benchmark as CUT. Figure 6, depicts the functional testing process of the CUT and the simulation results. After the simulation and synthesis of the design, post-layout simulation was generated (refer to Figure 7) using the Cadence RTL Encounter tool using the algorithm (Algorithm 1). This is stepwise procedure. Using the developed algorithmic procedure, we can generate layouts and extract the die size before sending to fabrication of chip

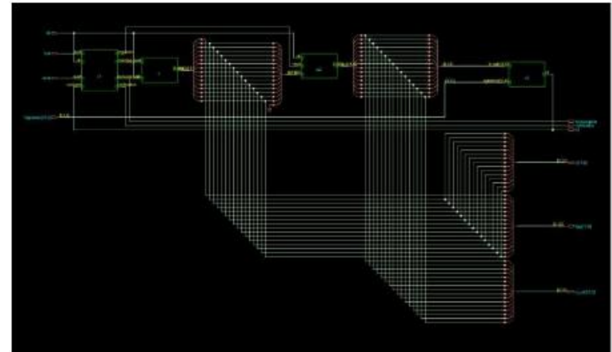

Fig. 5. Schematic view of the used modified BIST structure.

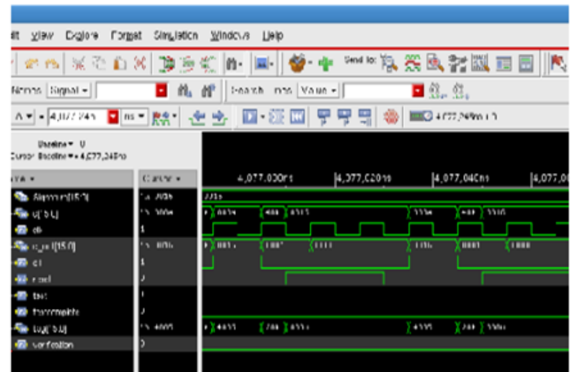

Fig. 6. Simulation results of the functional testing of the CUT

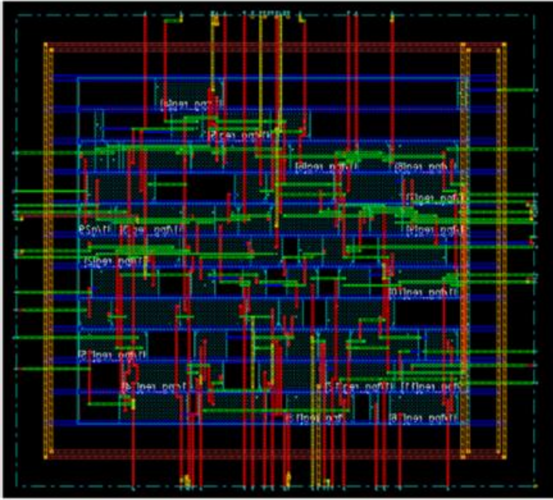

Fig. 7. The design's post-layout simulation

A. Algorithm 1:

- Write hdl topmodule > /root/Desktop/topmodule syn.v
- Write sdc > adder.sdc
- Ctrl+z
- Copy the file from desktop and paste in cadence tools/NCO/rclabs/work
- Then type "encounter" //new window will open
- Go to File → import design → verilogfile → browse, select topmodule syn.v
- File and add,
- In lef files → browse → back → lef → select all.lef and add then select top cell click on auto design
- Timing libraries ../lib/''slow''.lib ../lib/''fast''.lib
- In power type VDD and VSS
- Then in floorplan select specify floorplan
- Select aspect ratio as 30 to all corners
- In floorplan select automatic floorplan and select plan design ok
- In power → power planning click on add rings
- Select top and bottom layer as metal 5, left and right as metal 6,
- Select offset as center in channel and click ok
- Again in power → power planning click add stripes, select metal layer as metal 6
- In route click on special route, click ok for default settings
- For placement: Placement → place standard cell // layout will be generated
- Go to create rule and find the Die-Size of Design

B. FPGA vs ASIC

Table 2 shows the comparison of the obtained experimental results of the clock frequency and longest path delay of FPGA and ASIC implementations. Results shows that ASIC operating clock frequency is 1282 MHz that is quite high in comparison to FPGA. Last row of the table shows the die size requirements for ASIC implementation.

Table 2. Comparison FPGA vs ASIC

Process	Parameters		
	Frequency MHz	Longest Path Delay (ns)	Die size (mm)
FPGA	134	7,43	-
ASIC	1282	0.78	1053.96x1028.54

V. CONCLUSION

The Verilog code for 16-bit, maximal and bit-swapping LFSR has been synthesized through the set experiment. Using Cadence - tool, the implementation processes were successfully carried out on ASIC platform using 180 nm technology. The generated schematic and layout were recorded. The layout has undergone Design Rule Check (DRC) and the LVS (Layout vs Schematic) has been done to authenticate the layout. Initially, the design was implemented on FPGA platform. Through experiment we observed that operation that the operation frequency restricted with the limit to 134 MHz only. The same design was implemented on ASIC platform using 180 nm technology. The maximum LFSR and bit swapping LFSR was implemented on ASIC platform using 180 nm technology. We observe that the maximum frequency of 1282 MHz is achieved with a longest path delay of 780 ns.

It has been found that ASIC based design approach for Logic BIST based on LFSRs are very efficient and cost effective for large volume and size.

Therefore, it can be concluded that ASIC based design is preferable for complex and large volume applications than the designs based on FPGAs and Programmable Digital Signal Processors (PDSPs). In future many number of LFSRs of various lengths

can be implemented in a single ASIC with a best available technology and frequency of operation may improve the performance to meet the testing of sequential logic, complex SOCs and Analog mixed designs' testing requirements.

Coupled with the selection of processing unit in terms of low power dissipation of VLSI circuits of Embedded Vision System (EVS), could further reduce the power.

ACKNOWLEDGMENT

The acknowledgements are due to Authorities of Sultan Qaboos University (Sultanate of Oman) for providing generous research support grants and environments for carrying out the research works. This research work was supported by the internal grant of Sultan Qaboos University (number IG/ENG/ECED/20/01).

REFERENCES

[1] A. Ahmad, "Reliable and fault tolerant systems on chip through design for testability," in *Proc. 2019 Amity International Conference on Artificial Intelligence – (AICAI'19)*, Dubai, UAE, Feb. 4-7, 2019, pp. 50-53.

[2] A. Ahmad, "Automotive semiconductor industry – trends, safety and security challenges," in *Proc. 8th International Conference on Reliability, Infocom Technologies and Optimization (Trends and Future Directions) (ICRITO), Noida, India,* June 2020, pp. 1373-1377.

[3] S. Wang and S. K. Gupta, "A BIST TPG for low switching activity," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, vol. 21, no. 7, 2002, pp. 834-843.

[4] A. S. Abu-Issa and S. F. Quigley, "Bit- swapping LFSR and scan-chain ordering: a novel technique for peak and average- power reduction in scan-based BIST," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems,* vol. 28, no. 5, 2009, pp. 755-759.

[5] A. S. Abu-Issa, "Energy efficient scheme for multiple scan chains BIST using weight based segmentation," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 65, no. II(3), 2018, pp. 361-365.

[6] M. Nourani, M. Tehranipoor and N. Ahmed, "Low-transition test pattern generation for BIST based applications," *IEEE Trans. Computers*, vol. 57, no, 3, 2008, pp. 303-315.

[7] S. Wang and S. K. Gupta, "LT-RTPG: a new test per scan BIST TPG for low switching activity," *IEEE Trans. CAD*. vol. 25, 2006 (Aug), pp. 1565-1574.

[8] S. Hussain, M. A. Raheem and A. Ahmad, "SIC-TPG for path delay fault detection in VLSI circuits using scan insertion method," in *Proc. International Conference Devices for Integrated Circuit (DevIC)*, Kalyani, India, 2021, pp. 284-288.

[9] A. Ahmad, D. Al-Abri and S. S. Al-Busaidi, "Adding pseudo-random test sequence generator in the test simulator for DFT approach," *Journal Computer Technology and Applications*, *David Publishing (USA)*, vol. 3, no. 7, 2012, pp. 463-470.

[10] A. Ahmad and D. Ruelens, "Development of digital logic design teaching tool using MATLAB & SIMULINK," *IEEE Technology and Engineering Education (ITEE)*, vol. 8, no. 1, 2013, pp. 7-11.

[11] A. Ahmad A. and A. Al-Maashri, "Investigating some special sequence length generated through an external exclusive-NOR type LFSRs," *International Journal Electrical and Computer Engineering, (PERGAMON, Elsevier Science)*, vol. 34, no. 1, 2008, pp. 270-280.

[12] A. Al-Maashri and A. Ahmad, "Synthesis of a Fibonacci LFSR structure for FPGAs," in *Proc. of 3rd International Scientific Research and Innovation Congress, International Science and Art Research Centre (isarc) - Scientific Development and Innovative Approach*, Istanbul, Turkey, Aug. 26-27, 2022, pp. 845-853.